ATS860
250 MS/s 8-Bit PCI Digitizer

- 2 channels sampled at 8-Bit resolution
- 250 MS/s simultaneous real-time sampling rate on each input
- ±20 mV to ±10 V input range
- Up to 256 Million samples of on-board acquisition memory per channel
- Optional Dual Port Memory for data streaming
- AlazarDSO Oscilloscope Software
- Software Development Kit supports C/C++, C#, Python, MATLAB®, LabVIEW®
- Support for Windows & Linux

RoHS 2 COMPLIANT 2011/65/EU

CE

Product	Bus	Operating System	Channels	Sampling Rate	Bandwidth	Memory Per Channel	Resolution
ATS860	PCI 32 bit 33 MHz	Windows Linux 32-bit/64-bit	2	250 MS/s to 1 KS/s	100 MHz	Up to 256 Msamples	8 bits

Overview

ATS860 is a state of the art, dual-channel, high resolution, 8 bit, 250 MS/s waveform digitizer card for PCI bus, capable of storing up to 256 Million samples per channel of acquired data in its on-board memory.

With optional Dual Port Memory and fully asynchronous DMA, ATS860 allows users to build Windows or Linux based real-time data acquisition systems. Users are allowed to read acquired data even while the acquisition is in progress, including the ability to stream data to disk at rates up to 100 MS/s on one channel and 50 MS/s on 2 channels, simultaneously.

For scientific customers who want to record multiple analog inputs simultaneously, ATS860 offers multi-channel data acquisition systems of up to 8 channels.

ATS860 is supplied with AlazarDSO oscilloscope software that lets the user get started immediately without having to write any software.

Users who need to integrate the ATS860 in their own program can purchase a software development kit, ATS-SDK, for C/C++, C#, Python, MATLAB, and LabVIEW for both Windows and Linux operating systems.

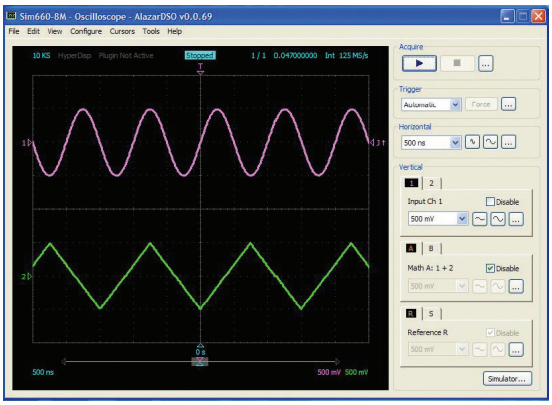
All of this advanced functionality is packaged in a low power, half-length PCI card.

Applications

Ultrasonic & Eddy Current NDT/NDE

Terabyte Storage Oscilloscope

Multi-Channel Transient Recording



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Analog Input
An ATS860 features two analog input channels with extensive functionality. Each channel has 100 MHz of full power analog input bandwidth. With software selectable attenuation, you can achieve an input voltage range of ±20 mV to ±10 V. Attenuating probes (sold separately) can extend the voltage range even higher.

Software selectable AC or DC coupling further increases the signal measurement capability. Software selectable 50 Ω input impedance makes it easy to interface to high speed RF signals.

For applications that require the best signal integrity, an Amplifier Bypass Mode is available as a standard feature. This feature improves harmonic distortion, leaving the input range fixed at a nominal value of ±500 mV.

Acquisition System
ATS860 PCI digitizers use a pair of state of the art 250 MS/s, 8-bit ADCs to digitize the input signals. The real-time sampling rate ranges from 250 MS/s down to 1 KS/s. The two channels are guaranteed to be simultaneous, as they share the exact same clock.

An acquisition can consist of multiple records, with each record being captured as a result of one trigger event. A record may contain both pre-trigger and post-trigger data.

Up to 256,000 triggers can be captured into on-board memory. There is no limit on number of triggers if dual port memory is used to acquire data.

In between the multiple triggers being captured, the acquisition system is re-armed by the hardware within 64 sampling clock cycles.

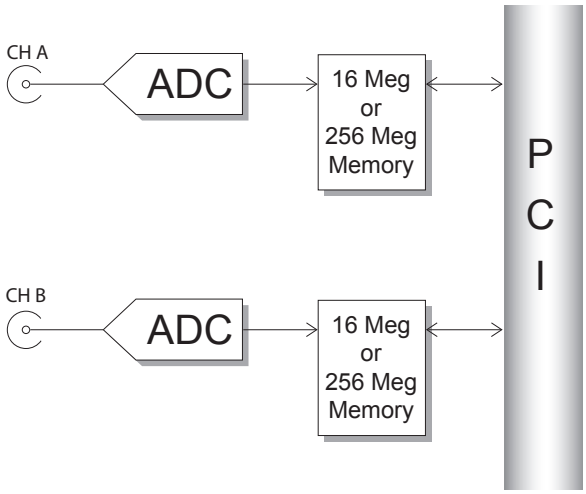
This mode of capture, sometimes referred to as Multiple Record, is very useful for capturing data in applications with a very rapid or unpredictable trigger rate. Examples of such applications include medical imaging, ultrasonic testing, NMR spectroscopy and lightning test.

On-Board Acquisition Memory
The standard ATS860 PCI digitizer features 16 Million points of acquisition memory for each channel.

Acquisition memory can optionally be upgraded to provide 256 Million samples per channel of signal storage.

Data is acquired into the onboard memory before being transferred to the host PC memory. This transfer is performed using Direct Memory Access (DMA), which uses scatter-gather bus mastering technology.

By default, on-board memory is single-ported. If dual port memory is needed, it must be purchased as a separate line item.



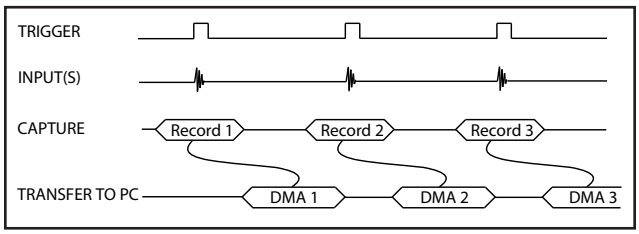
Optional Dual Port Memory
Optionally, ATS860 can be equipped with dual port acquisition memory. This means that data can be transferred to host PC memory even if an acquisition is in progress.

Other digitizers on the market do not provide dual-port memory, thus prolonging the re-arm time of the digitizer. This limits the maximum trigger repeat rate they can handle in applications involving fast triggers, such as OCT, medical imaging, ultrasonic testing, NMR spectroscopy and other pulse-echo testing methodologies.

ATS860, equipped with Dual Port Memory option, does not suffer from such drawbacks and provides the best solution for these applications.

AlazarTech has designed custom memory management circuitry to interface this dual port memory to PCI bus. This circuitry is called AutoDMA, which can work in many different modes.

Traditional AutoDMA
In order to acquire both pre-trigger and post-trigger data in a dual-ported memory environment, users can use Traditional AutoDMA.



Data is returned to the user in buffers, where each buffer can contain from 1 to 8192 records (triggers). This number is called RecordsPerBuffer.

Users can also specify that each record should come with its own header that contains a 40-bit trigger timestamp.

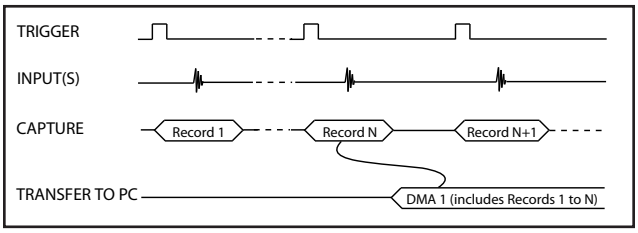
A BUFFER_OVERFLOW flag is asserted if more than 512 buffers have been acquired by the acquisition system, but not transferred to host PC memory by the AutoDMA engine.

While Traditional AutoDMA can acquire data to PC host memory at sustained rates in excess of 100 MB/s, an overflow can occur if more than 512 triggers occur in very rapid succession, even if all the on-board memory has not been used up.

No Pre-Trigger (NPT) AutoDMA

Many ultrasonic scanning and medical imaging applications do not need any pre-trigger data: only post-trigger data is sufficient.

NPT AutoDMA is designed specifically for these applications. By only storing post-trigger data, the memory bandwidth is optimized and the entire on-board memory acts like a very deep FIFO.



Note that a DMA is not started until RecordsPerBuffer number of records (triggers) have been acquired.

NPT AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

More importantly, a BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up. This provides a very substantial improvement over Traditional AutoDMA.

NPT AutoDMA can easily acquire data to PC host memory at sustained rates in excess of 100 MB/s without causing an overflow.

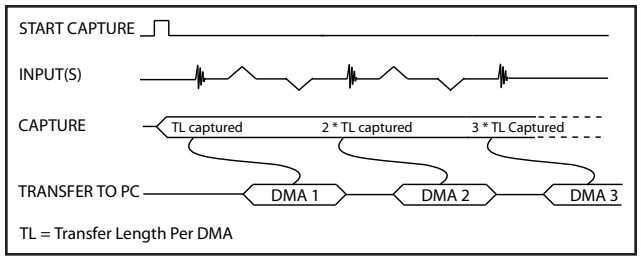
This is the recommended mode of operation for most ultrasonic scanning, OCT and medical imaging applications.

Continuous AutoDMA

Continuous AutoDMA is also known as the data streaming mode.

In this mode, data starts streaming across the PCI bus as soon as the ATS860 is armed for acquisition. It is important to note that triggering is disabled in this mode.

Continuous AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.



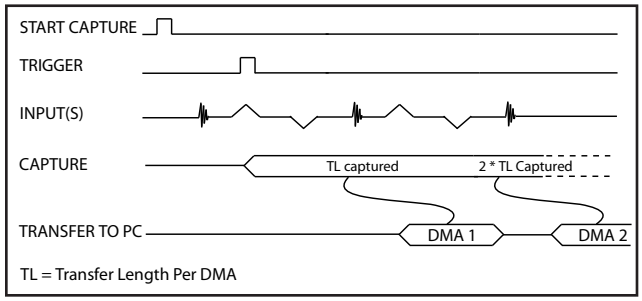
A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

The amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Continuous AutoDMA can easily acquire data to PC host memory at sustained rates in excess of 100 MB/s without causing an overflow. This is the recommended mode for very long signal recording.

Triggered Streaming AutoDMA

Triggered Streaming AutoDMA is virtually the same as Continuous mode, except the data transfer across the bus is held off until a trigger event has been detected.



Triggered Streaming AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

As in Continuous mode, the amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Triggered Streaming AutoDMA can easily acquire data to PC host memory at sustained rates in excess of 100 MB/s without causing an overflow. This is the recommended mode for RF signal recording that has to be started at a specific time, e.g. based on a GPS pulse.

Asynchronous DMA

AlazarTech's dual port memory and AutoDMA circuit maximize throughput at the hardware level. An equally sophisticated software architecture is required to allow a Windows or Linux based application program to take advantage of this throughput despite all the bottlenecks created by the operating system.

AlazarTech calls this architecture Asynchronous DMA or AsyncDMA.

AsyncDMA uses overlapped IO to re-start DMAs and consume data, thereby minimizing CPU usage to almost 0%, reducing re-arm time of DMAs and allowing the full bus bandwidth to be realized.

Another advantage of AsyncDMA is that it can provide the full bus bandwidth to a multi-card Master/Slave system.

Some helper routines are provided for programming languages that cannot directly use overlapped IO. Examples of such languages include Visual BASIC and LabVIEW.

It is important to note that AsyncDMA is a software construct and it can be used with any of the AutoDMA modes mentioned before.

Software Selectable Bandwidth Limit

A majority of applications for PCI digitizers require oversampling of input signal, i.e. the frequency of the analog signal being digitized is a factor of 5 or 6 lower than the sample rate or even the Nyquist rate.

ATS860 features a software-controlled bandwidth limit switch, which reduces high frequency noise and improves signal to noise ratio. This switch is independently selectable for each input channel.

When selected, bandwidth limit switch can reduce the input bandwidth of a particular input to be approximately 20 MHz.

Amplifier Bypass Mode

To obtain optimum dynamic performance, choose the Amplifier Bypass Mode.

Each channel can be independently bypassed using on-board DIP-switches.

Once the amplifier has been bypassed, the input for that channel has 50 Ω impedance, DC coupling and a 500 mV full scale input range. Diode protection is still included, but users should avoid saturation of the input beyond 120% of full scale.

Triggering

The ATS860 is equipped with sophisticated digital triggering options, such as programmable trigger thresholds and slope on any of the input channels or the External Trigger input.

While most oscilloscopes offer only one trigger engine, ATS860 offers two trigger engines (called Engines X and Y). This allows the user to combine the two engines using a logical OR, AND or XOR operand.

The user can specify the number of records to capture in an acquisition, the length of each record and the amount of pre-trigger data.

A programmable trigger delay can also be set by the user. This is very useful for capturing the signal of interest in a pulse-echo application, such as ultrasound, radar, lidar etc.

Trigger Time Stamp

A 40-bit time stamp counter comes standard with the ATS860. By default, this counter is initialized to a zero value when an acquisition session is started and increments once for every two samples captured, thus providing a 4-clock timing accuracy. At 250 MS/s sample rate, this counter will not roll over for well over 2 hours.

The value of this counter is latched into trigger memory for each trigger, i.e. once per record, for up to specified number of records.

This allows the user to find out the timing of each trigger in a multiple record acquisition relative to the start of the acquisition.

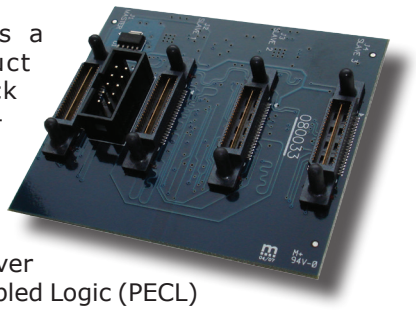
It is also possible to configure the timestamp counter to reset for the first acquisition only and never again, until a software reset is issued. This feature enables users to obtain precise timing information about multiple acquisitions.

Multiple-Digitizer Synchronization

ATS860 features a Master/Slave connector that allows synchronization of multiple digitizers to allow truly synchronous sampling across as many as 8 channels.

A SyncBoard 860 (sold separately) is required to connect the Master/Slave connectors on multiple digitizers in the system together. Such a system is called a Master/Slave system.

SyncBoard 860 is available for 2 board synchronization and 4 board synchronization.



SyncBoard 860 is a board-level product that features clock buffering, clock distribution, trigger resynchronization and controlled impedance, equal length traces to deliver Positive Emitter Coupled Logic (PECL) level clock, trigger and initialization signals to each ATS860 in the system.

A Master/Slave system is guaranteed to sample simultaneously across all channels in that system. Triggering is also guaranteed to be simultaneous across all digitizers in the system, i.e. all boards will trigger on the same clock edge.

ATS860 based master/slave systems provide the best price-performance for high channel count systems.

Optional External Clock

While the ATS860 features a low jitter, high reliability 250 MHz oscillator as the timebase source, there are occasions when ATS860 has to be synchronized to an external clock source.

ATS860 External Clock option provides an SMA input for an external clock signal, which can be a sine wave or LVTTL signal.

User can set the input impedance and coupling for the external clock input by setting the appropriate DIP switches located in the top-left corner of the ATS860 printed circuit board.

In order to operate the ADC under optimal conditions, the user must set the appropriate frequency range for the external clock being supplied. The following ranges are supported:

Fast External Clock: 20 MHz < fEXT < 250 MHz

Slow External Clock: fEXT < 40 MHz

The active edge of the external clock is software selectable between the rising or falling edge.

Slow External Clock

ATS860 uses ADC converters that cannot operate below 20 MHz clock frequency. For customers who have clocks that are slower than 20 MHz, AlazarTech has designed the powerful Slow External Clock.

Slow External Clock must be a 3.3 Volt LVTTL signal. Sine wave or other types of signals are not allowed.

In this mode, the ADCs run at 125 MHz internal frequency, but the hardware detects a rising (or falling) edge of the incoming Slow External Clock and latches one sample point for each edge. This results in a sampling jitter of ±8 ns, which may or may not be acceptable in a particular application.

Trigger Output

ATS860 provides Trigger Output capability. This feature uses the TRIG OUT BNC connector to output a TTL signal synchronous to the ATS860 Trigger signal, allowing users to synchronize their test systems to the ATS860 Trigger.

When combined with the Trigger Delay feature of the ATS860, this option is ideal for ultrasonic and other pulse-echo imaging applications.

Calibration

Every ATS860 digitizer is factory calibrated for gain and offset accuracy to NIST-traceable standards, using a Fluke 5820A oscilloscope calibrator. To recalibrate an ATS860, the digitizer must either be shipped back to the factory or a qualified metrology laboratory.

RoHS Compliance

ATS860 units built after June 2007 are fully RoHS compliant, as defined by Directive 2011/65/EU (RoHS 2) of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

All manufacturing is done using RoHS-compliant components and lead-free soldering.

AlazarDSO Software

ATS860 is supplied with the powerful AlazarDSO software that allows the user to setup the acquisition hardware and capture, display and archive the signals.

The Stream-To-Memory command in AlazarDSO allows users to stream a large dataset to motherboard memory.

AlazarDSO software also includes powerful tools for benchmarking the computer bus and disk drive.

Software Development Kits

AlazarTech provides easy to use software development kits for customers who want to integrate the ATS860 into their own software.

A Windows and Linux compatible software development kit, called ATS-SDK, includes headers, libraries and source code sample programs written in C/C++, C#, Python, MATLAB, and LabVIEW. These programs can fully control the ATS860 and acquire data in user buffers.

Linux Support

AlazarTech offers ATS860 binary drivers for most of the popular Linux distributions, such as CentOS, Ubuntu,...

Users can download the binary driver for their specific distribution by choosing from the available drivers here:

ftp://release@ftp.alazartech.com/outgoing/linux

Also provided is a GUI application called AlazarFrontPanel that allows simple data acquisition and display.

ATS-SDK includes source code example programs for Linux, which demonstrate how to acquire data programmatically using a C compiler.

If customers want to use ATS860 in any Linux distribution other than the one listed above, they can have the AlazarTech engineering team generate an appropriate driver for a nominal fee, if applicable.

Based on a minimum annual business commitment, the Linux driver source code license (order number ATS860-LINUX) may be granted to qualified OEM customers for a fee. For release of driver source code, a Non-Disclosure Agreement must be executed between the customer's organization and AlazarTech.

All such source code disclosures are made on an as-is basis with limited support from the factory.

Export Control Classification

According to the Export Controls Division of Government of Canada, ATS860 is currently not controlled for export from Canada. Its export control classification is N8, which is equivalent to ECCN EAR99. ATS860 can be shipped freely outside of Canada, with the exception of countries listed on the Area Control List and Sanctions List. Furthermore, if the end-use of ATS860, in part or in its entirety, is related to the development or deployment of weapons of mass destruction, AlazarTech is obliged to apply for an export permit.

EC Conformity

ATS860 conforms to the following standards:

Electromagnetic Emissions:
CISPR 22:2006/EN 55022:2006 (Class A):
Information Technology Equipment (ITE). Radio disturbance characteristics. Limits and method of measurement.

Electromagnetic Immunity:
CISPR 24:1997/EN 55024:1998 (+A1 +A2):
Information Technology Equipment Immunity characteristics — Limits and methods of measurement.

Safety:
IEC 60950-1:2005: Information technology equipment — Safety — Part 1: General requirements.

IEC 60950-1:2006: Information technology equipment — Safety — Part 1: General requirements.

ATS860 also follows the provisions of the following directives: 2006/95/EC (Low Voltage Equipment); 2004/108/EC (Electromagnetic Compatibility).

FCC & ICES-003 Compliance

ATS860 has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15, subpart B of the FCC Rules, and the Canadian Interference-Causing Equipment Standard ICES-003:2004.

ATS860
250 MS/s 8-Bit PCI Digitizer

System Requirements

Personal computer with at least one free PCI slot, 512 MB RAM, 100 MB of free hard disk space

Power Requirements

+5 V	2.4 A, typical for ATS860-8M 3.1 A, typical for ATS860-128M
	+5 V voltage level must remain between the range of 4.75 V to 5.20 V at all times after power-on

Physical

Size	Single slot, half length PCI card (4.2 inches x 7.2 inches)
Weight	500 g

I/O Connectors

CH A, CH B, TRIG IN, TRIG OUT	BNC female connectors
ECLK	SMA female connector

Environmental

Operating temperature	0 to 55 degrees Celsius
Storage temperature	-20 to 70 degrees Celsius
Relative humidity	5 to 95%, non-condensing

Acquisition System

Resolution	8 bits
Bandwidth (-3 dB)	
DC-coupled, 1 MΩ	DC - 65 MHz
DC-coupled, 50 Ω	DC - 100 MHz
AC-coupled, 1 MΩ	10 Hz - 65 MHz
AC-coupled, 50 Ω	100 kHz - 100 MHz
Bandwidth flatness:	± 1 dB
Number of channels	2, simultaneously sampled
Maximum Sample Rate	250 MS/s single shot
Minimum Sample Rate	1 KS/s single shot for internal clocking
Full Scale Input ranges	
1 MΩ input impedance:	±20 mV, ±40 mV, ±50 mV, ±80 mV, ±100 mV, ±200 mV, ±400 mV, ±500 mV, ±800 mV, ±1 V, ±2 V, ±4 V, ±5 V, ±8 V, and ±10 V, software selectable
50 Ω input impedance:	±20 mV, ±40 mV, ±50 mV, ±80 mV, ±100 mV, ±200 mV, ±400 mV, ±500 mV, ±800 mV, ±1 V, ±2 V, and ±4 V, software selectable
DC accuracy	±2% of full scale in all input ranges
Input coupling	AC or DC, software selectable
Input impedance	50 Ω or 1 MΩ ±1% in parallel with 50 pF ±10 pF, software selectable
Input protection	
1 MΩ	±28V (DC + peak AC for CH A, CH B and EXT only without external attenuation)
50 Ω	±4V (DC + peak AC for CH A, CH B and EXT only without external attenuation)

Amplifier Bypass Mode

Standard Feature	Yes
DIP Switch selectable	Yes, independently for each channel
Input Range	Approx. 500 mV rms
Input Coupling	DC, irrespective of the input coupling setting for the channel
Input Impedance	50 Ω, irrespective of the input impedance setting for the channel
Input bandwidth (-3 dB)	100 MHz

On-Board Acquisition Memory System

Onboard acq memory	32 MB for ATS860-8M 512 MB for ATS860-128M
Acquisition Memory/ch	Up to 16 Million samples per channel for ATS860-16M Up to 256 Million samples per channel for ATS860-256M
Record Length	Software selectable with 32 point resolution. Record length must be a minimum of 256 points. Maximum record length is limited by the acquisition memory per channel.
Number of Records	Software selectable from a minimum of 1 to a maximum of 256,000 or (Acquisition Memory Per Channel / (Record Length+16)), whichever is lower
Pre-trigger depth	0 to (Record Length-128), software selectable with 32 point resolution
Post-trigger depth	Record Length - Pre-trigger depth

Timebase System

Timebase options	Internal Clock or External Clock (Optional)
Internal Sample Rates	250 MS/s, 125 MS/s, 50 MS/s, 25 MS/s, 10 MS/s, 5 MS/s, 2 MS/s, 1 MS/s, 500 KS/s, 200 KS/s, 100 KS/s, 50 KS/s, 20 KS/s, 10 KS/s, 5 KS/s, 2 KS/s, 1 KS/s
Internal Clock accuracy	±25 ppm

Dynamic Parameters

Typical values measured using a randomly selected ATS860 with Amplifier Bypass Mode. Input was provided by a HP8656A signal generator, followed by a 9-pole, 1 MHz band-pass filter (TTE Q36T-1M-100K-50-720B). Input frequency was set at 1 MHz and output amplitude was 500 mV rms, which is approximately 95% of the 525 mVrms full scale input in Amplifier Bypass Mode.

SNR	44.5 dB
SINAD	41.2 dB
THD	-50.1 dB
SFDR	-47.4 dB

Note that these dynamic parameters may vary from one unit to another, with input frequency and with the full scale input range selected.

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Optional ECLK (External Clock) Input

Signal Level	±500 mV Sine wave or 3.3 V LVTTL
Input impedance	50 Ω or 1 kΩ, selectable
Maximum frequency	250 MHz for Fast External Clock 40 MHz for Slow External Clock
Minimum frequency	20 MHz for Fast External Clock DC for Slow External Clock
Decimation factor	Software selectable from 1 to 100,000
Sampling Edge	Rising or Falling, software selectable

Triggering System

Mode	Edge triggering with hysteresis
Comparator Type	Digital comparators for internal (CH A, CH B) triggering and analog comparators for TRIG IN (External) triggering
Number of Trigger Engines	2
Trigger Engine Combination	OR, AND, XOR, selectable
Trigger Engine Source	CH A, CH B, EXT, Software or None, independently software selectable for each of the two Trigger Engines
Hysteresis	±5% of full scale input, typical
Trigger sensitivity	±10% of full scale input range. This implies that the trigger system may not trigger reliably if the input has an amplitude less than ±10% of full scale input range selected
Trigger level accuracy	±5%, typical, of full scale input range of the selected trigger source
Bandwidth	100 MHz
Trigger Delay	Software selectable from 0 to 9,999,999 sampling clock cycles
Trigger Timeout	Software selectable with a 10 µs resolution. Maximum settable value is 3,600 seconds. Can also be disabled to wait indefinitely for a trigger event

TRIG IN (External Trigger) Input

Input impedance	1.01 MΩ ±10% in parallel with 50 pF ±10 pF
Bandwidth (-3 dB)	
DC-coupled	DC - 50 MHz
AC-coupled	10 Hz - 50 MHz
Input range	±5 V or ±1 V, software selectable
DC accuracy	±10% of full scale input
Input protection	±28 V (DC + peak AC without external attenuation)
Coupling	AC or DC, software selectable

TRIG OUT Output

Output Signal	5 Volt TTL
Synchronization	Synchronized to rising edge of sampling clock

Materials Supplied

ATS860 PCI Card

ATS860 Installation Disk (on USB Flash Drive)

Certification and Compliances

RoHS 2 (Directive 2011/65/EU) Compliance

CE Marking — EC Conformity

FCC Part 15 Class A / ICES-003 Class A Compliance

All specifications are subject to change without notice

ORDERING INFORMATION

ATS860-16M	ATS860-001
ATS860-256M	ATS860-010
ATS860: Dual Port Memory Upgrade	ATS860-002
ATS860: 16 Meg to 256 Meg Upgrade	ATS860-011
ATS860: External Clock Upgrade	ATS860-004
SyncBoard 860 2x	ATS860-006
SyncBoard 860 4x	ATS860-007
ATS860-16M: One Year Extended Warranty	ATS860-061
ATS860-256M: One Year Extended Warranty	ATS860-062
Software Development Kit (Supports C/C++, Python, MATLAB, and LabVIEW)	ATS-SDK

Manufactured By:

Alazar Technologies Inc.

6600 TRANS-CANADA HIGHWAY, SUITE 310
POINTE-CLAIRE, QC, CANADA H9R 4S2

TOLL FREE: 1-877-7-ALAZAR
TEL: (514) 426-4899 FAX: (514) 426-2723

E-MAIL: info@alazartech.com

DATASHEET REVISION HISTORY

Changes from version 1.2 (Oct 2013) to version 1.2A	Section, Page
Added Python to list of SDK supported languages, and Support for Windows & Linux	Features, pg. 1
Removed deprecated *Optional Data Streaming To Hard Disk*	Features, pg. 1
Changed maximum number of channels for multi-channel data acquisition systems to 8	Overview, pg. 1
Removed note on availability of special order item for higher channel counts	Overview, pg. 1
Added Python & LabVIEW to list of supported languages for ATS-SDK, removed ATS-VI	Overview, pg. 1
Removed *Stream To Disk*, product deprecated	Stream To Disk, pg. 4
Updated section on RoHS compliance	RoHS Compliance, pg. 5
Modified AlazarDSO description	AlazarDSO Software, pg. 5
Removed section *AlazarDSO Plug-Ins*; product deprecated	AlazarDSO Plug-Ins, pg. 5
New section *Software Development Kits* to replace sections: *ATS-SDK Software Development Kit* and *ATS-VI Software Development Kit*	Software Development Kits, pg. 5
Replaced section *ATS-Linux* with new *Linux Support* section	Linux Support, pg. 5
Added Export Control Classification information	Export Control Classification, pg. 6
Added section on EC Conformity	EC Conformity, pg. 6
Added section on FCC & ICES-003 Compliance	FCC & ICES-003 Compliance, pg. 6
Updated External Trigger Input Impedance to 1.01 MΩ ±10%	TRIG IN (External Trigger) Input, pg. 8
Updated list of Certification and Compliances	Certification and Compliances, pg. 8
Added products ATS860-061, ATS860-062	Ordering Information, pg. 8
Replaced product ATS860-SDK with ATS-SDK	Ordering Information, pg. 8
Removed product ATS860-VI (ATS-SDK now supports LabVIEW)	Ordering Information, pg. 8
Removed products ATS860-Linux, ATS-STR, ATS-DSO-PDK	Ordering Information, pg. 8