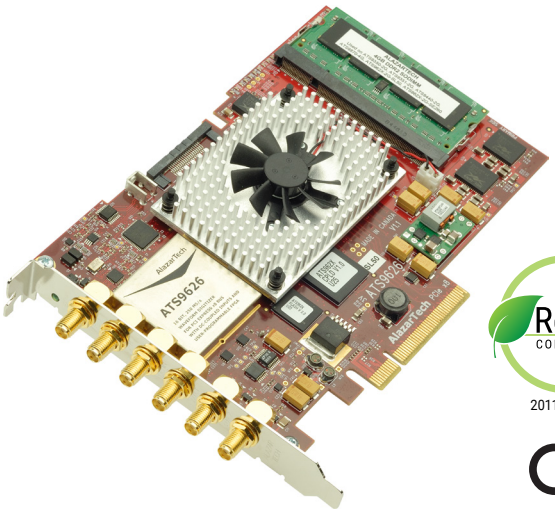
ATS9626

250 MS/s 16-Bit DC-coupled PCI Express Digitizer with user-programmable FPGA

- PCI Express (8-lane) interface
- 2 channels sampled at 16-bit resolution
- 250 MS/s real-time sampling rate
- User programmable Coprocessor FPGA
- 2 Gigasample dual-port memory buffer
- Continuous streaming mode
- DC-coupled inputs
- Asynchronous DMA device driver
- AlazarDSO oscilloscope software
- Software Development Kit supports C/C++, C#, Python, MATLAB®, LabVIEW®
- Linux driver available



RoHS 2 COMPLIANT 2011/65/EU

CE

Product	Bus	Operating System	Channels	Sampling Rate	Bandwidth	Memory Per Channel	Resolution
ATS9626	PCIe x8	Windows Linux 32-bit/64-bit	2	250 MS/s to 50 MS/s	DC-120 MHz	Up to 2 Gigasample	16 bits

Overview

ATS9626 is an 8-lane PCI Express (PCIe x8), dual-channel, high speed, 16 bit, 250 MS/s waveform digitizer card with dc-coupled inputs and an on-board, user-programmable FPGA, called a Coprocessor FPGA.

The Coprocessor FPGA is an Altera Stratix III device with on-chip memory, hardware multipliers, DSP blocks and a fast fabric that allows both integer based and floating point digital signal processing.

All data acquired by the on-board A/D converters flows through the Coprocessor FPGA, allowing user-defined FPGA circuit to process the data in real time and at hardware speed.

The main difference between ATS9626 and ATS9625 is input coupling: ATS9626 provides dc coupling, whereas ATS9625 provides ac coupling.

ATS9626 is supplied with AlazarDSO software that lets the user get started immediately without having to go through a software development process.

Users who want to design their own Coprocessor FPGA must purchase ATS9626 Coprocessor FPGA Development Kit (also called ATS9626-FDK).

Users who need to integrate the ATS9626 in their own program can purchase a software development kit, ATS-SDK, for C/C++, C#, Python®, MATLAB® and LabVIEW® for both Windows and Linux operating systems.

All of this advanced functionality is packaged in a low power, half-length PCI Express card.

Applications

Optical Coherence Tomography (OCT)

Radar/RF Signal Recording & Analysis

Ultrasonic & Eddy Current NDT/NDE

Terabyte Storage Oscilloscope

High Resolution Oscilloscope

Lidar

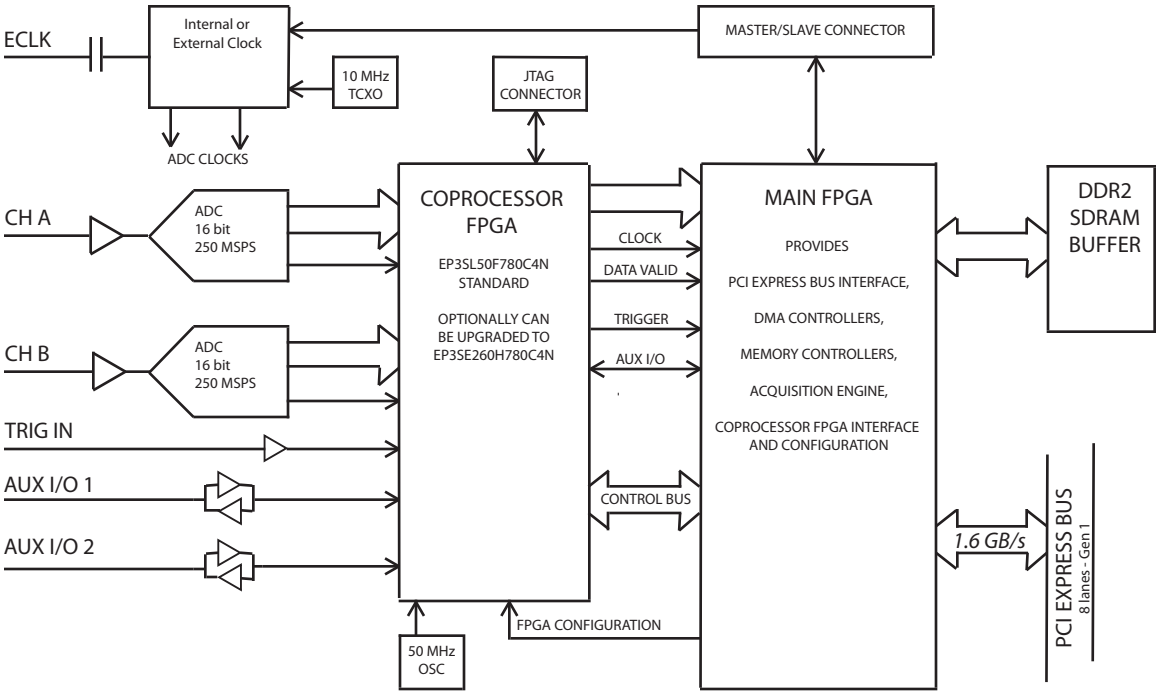
Spectroscopy

Digital Down Conversion (DDC)

Multi-Channel Transient Recording

ATS9626

250 MS/s 16-Bit DC-coupled PCI Express Digitizer with user-programmable FPGA



PCI Express Bus Interface

ATS9626 interfaces to the host computer using an 8-lane PCI Express bus. Each lane operates at 2.5 Gbps.

According to PCIe specification, an 8-lane board can be plugged into any 8-lane or 16-lane slot, but not into a 4-lane or 1-lane slot. As such, ATS9626 requires at least one free 8-lane or 16-lane slot on the motherboard.

The physical and logical PCIe x8 interface is provided by an on-board FPGA, which also integrates acquisition control functions, memory management functions and interface to Coprocessor FPGA. This very high degree of integration maximizes product reliability.

AlazarTech's bus benchmark has been proven on many computers, including workstation and server class machines from Dell and HP, as well as no-name machines built around motherboards from Intel, ASUS, Tyan, Supermicro etc.

Users must always be wary of throughput specifications from manufacturers of waveform digitizers. Some unscrupulous manufacturers tend to specify the raw, burst-mode throughput of the bus. Others mention data throughput rates to operating system kernel memory, not user accessible memory.

AlazarTech, on the other hand, specifies the benchmarked sustained throughput to buffers in user space.

To achieve such high throughput, a great deal of proprietary memory management logic and kernel mode drivers have been designed by AlazarTech.

Analog Input

ATS9626 has two dc-coupled analog input channels. Each channel has analog input bandwidth from DC to 120 MHz.

The full scale input range is fixed at ±1.25V.

For applications that require capture of small signals, customers can purchase the ATS9626-014 upgrade that allows the input range to be permanently changed to ±200mV. It should be noted that the analog input bandwidth is limited to 100 MHz with this upgrade.

Input impedance of both channels is fixed at 50Ω.

Acquisition System

ATS9626 PCI Express digitizers use state of the art 250 MSPS, 16-bit ADCs to digitize the input signals. The real-time sampling rate of the ADCs ranges from 250 MS/s down to 50 MS/s.

The two channels are guaranteed to be simultaneous, with a maximum clock skew of 10 ps. Additive jitter of the clock distributor circuit is less than 225 fs_{rms}.

An acquisition can consist of multiple records, with each record being captured as a result of one trigger event. A record can contain both pre-trigger and post-trigger data.

Infinite number of triggers can be captured by ATS9626, when it is operating using dual-port memory.

In between the multiple triggers being captured, the acquisition system is re-armed by the hardware within 256 sampling clock cycles.

This mode of capture, sometimes referred to as Multiple Record, is very useful for capturing data in applications with a very rapid or unpredictable trigger rate. Examples of such applications include medical imaging, ultrasonic testing, OCT and NMR spectroscopy.

Coprocessor FPGA

ADC data flows through the Coprocessor FPGA before it is stored in the on-board memory or transferred to host PC memory.

Programming the Coprocessor FPGA involves a design flow that revolves around Quartus II software from Altera Corporation. An FPGA programmer can use VHDL or Verilog or even schematic-based design entry and then compile the design, a process that generates a downloadable FPGA binary file.

ModelSim simulator can be used to do functional simulation to verify the design.

Alternately, the FPGA can be designed in MATLAB Simulink environment and DSP Builder software from Altera can be used to bring the design into Quartus II, where compilation can take place.

It should be noted that the ATS962x-FDK (ATS962x Coprocessor FPGA Development Kit) offered by AlazarTech (and sold separately) offers example projects in VHDL source code only.

Downloading a new FPGA binary file into the Coprocessor FPGA is very quick and easy. The download process takes approximately 125 milliseconds for the standard Coprocessor FPGA.

By pre-processing the ADC data in the Coprocessor FPGA, users can customize the entire personality of the ATS9626.

Some examples of Coprocessor FPGAs are: decimating filter for protection against anti-aliasing; digital receivers using a programmable NCO; Optical Coherence Tomography signal processing using FFTs; autocorrelation circuit for lidar applications; hardware averaging for spectroscopy applications ...

Optional High Capacity Coprocessor FPGA

The standard Coprocessor FPGA is an Altera Stratix III EP3SL50F780C4N device. For some users, this FPGA may not have enough resources to implement their entire design.

In such situations, it is possible to order the ATS9626 with a Coprocessor Upgrade to EP3SE260H780C4N FPGA.

Note that orders for high capacity FPGA may have a significant lead-time.

On-Board Acquisition Memory

ATS9626 supports on-board memory buffers of 2 Gigasamples.

Acquisition memory can either be divided equally between the two input channels or devoted entirely to one of the channels.

The main advantage of having on-board memory is that it acts as a very deep FIFO between the Analog to Digital converters and PCI Express bus, allowing very fast sustained data transfers across the bus, even if the operating system or another motherboard resource temporarily interrupts DMA transfers.

Maximum Sustained Transfer Rate

PCI Express support on different motherboards is not always the same, resulting in significantly different sustained data transfer rates. The reasons behind these differences are complex and varied and will not be discussed here.

ATS9626 users can quickly determine the maximum sustained transfer rate for their motherboard by inserting their card in a PCIe slot and running the Tools:Benchmark:Bus tool provided in AlazarDSO software.

ATS9626, which is equipped with dual-port on-board memory, will be able to achieve this maximum sustained transfer rate.

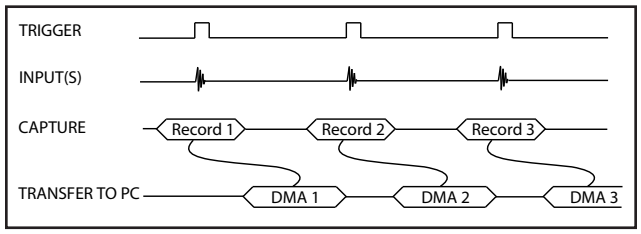
Recommended Motherboards

Many different types of motherboards have been benchmarked by AlazarTech. The motherboard that has consistently given the best throughput results (as high as 1.7 GB/s) has been the ASUS P6T7 and the new P9X79 Pro.

Older motherboards, such as Intel S5000PSLSATA that use the S5000 chipset also provide very good throughput.

Traditional AutoDMA

In order to acquire both pre-trigger and post-trigger data in a dual-ported memory environment, users can use Traditional AutoDMA.



Data is returned to the user in buffers, where each buffer can contain from 1 to 8191 records (triggers). This number is called RecordsPerBuffer.

Users can also specify that each record should come with its own header that contains a 40-bit trigger timestamp.

A BUFFER_OVERFLOW flag is asserted if more than 512 buffers have been acquired by the acquisition

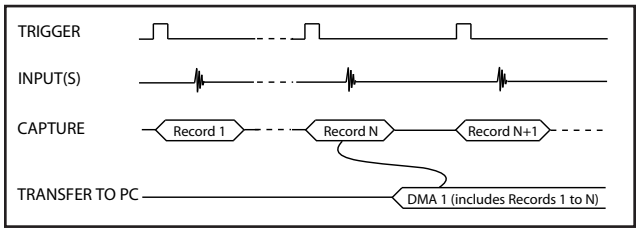
system, but not transferred to host PC memory by the AutoDMA engine.

In other words, a BUFFER_OVERFLOW can occur if more than 512 triggers occur in very rapid succession, even if all the on-board memory has not been used up.

No Pre-Trigger (NPT) AutoDMA

Many ultrasonic scanning and medical imaging applications do not need any pre-trigger data: only post-trigger data is sufficient.

NPT AutoDMA is designed specifically for these applications. By only storing post-trigger data, the memory bandwidth is optimized and the entire on-board memory acts like a very deep FIFO.



Note that a DMA is not started until RecordsPerBuffer number of records (triggers) have been acquired and written to the on-board memory.

NPT AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

More importantly, a BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up. This provides a very substantial improvement over Traditional AutoDMA.

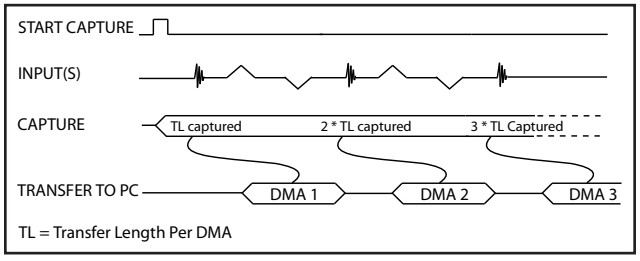
NPT AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow.

This is the recommended mode of operation for most ultrasonic scanning, OCT and medical imaging applications.

Continuous AutoDMA

Continuous AutoDMA is also known as the data streaming mode.

In this mode, data starts streaming across the PCI Express bus as soon as the ATS9626 is armed for acquisition. It is important to note that triggering is disabled in this mode.



Continuous AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

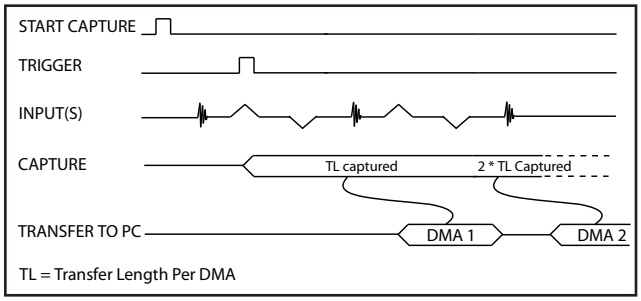
A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

The amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Continuous AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for very long signal recording.

Triggered Streaming AutoDMA

Triggered Streaming AutoDMA is virtually the same as Continuous mode, except the data transfer across the bus is held off until a trigger event has been detected.



Triggered Streaming AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

As in Continuous mode, the amount of data to be captured is controlled by counting the number of buffers acquired.

Acquisition is stopped by an AbortCapture command.

Triggered Streaming AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow.

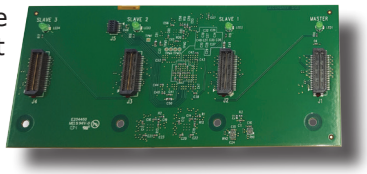
This is the recommended mode for RF signal recording that has to be started at a specific time, e.g. based on a GPS pulse.

Master/Slave Systems

Users can create a multi-board Master/Slave system by synchronizing up to four ATS9626 boards using an appropriate SyncBoard-9626.

SyncBoard-9626 is a mezzanine board that connects to the Master/Slave connector along the top edge of the ATS9626 and sits parallel to the motherboard. For additional robustness, users can secure the SyncBoard-9626 to a bracket mounted on each of the ATS9626 boards.

SyncBoard-9626 is available in different widths:2X, 4X, 2X-W, 3X-W or 4X-W.



SyncBoards with the -W suffix provide 2-slot spacing between ATS9626 cards to support some of the newer motherboards that space out the on-board x8 or x16 slots by two slots. The -W SyncBoards are also a better solution from thermal point of view, as there is better air flow with 2-slot spacing.

The 2X and 2X-W models allows a 2-board Master/Slave system; the 3X-W model allows a 2 or 3-slot Master/Slave system; and the 4X and 4X-W models allow 2, 3 or 4 board Master/Slave systems.

The Master board's clock and trigger signals are copied by the SyncBoard-9626 and supplied to all the Slave boards. This guarantees complete synchronization between the Master board and all Slave boards.

It should be noted that SyncBoard-9626 does not use a PLL-based clock buffer, allowing the use of variable frequency clocks in Master/Slave configuration.

A Master/Slave system samples all inputs simultaneously and also triggers simultaneously on the same clock edge.

Asynchronous DMA Driver

The various AutoDMA schemes discussed above provide hardware support for optimal data transfer. However, a corresponding high performance software mechanism is also required to make sure sustained data transfer can be achieved.

This proprietary software mechanism is called Async DMA (short for Asynchronous DMA).

A number of data buffers are posted by the application software. Once a data buffer is filled, i.e. a DMA has been completed, ATS9626 hardware generates an interrupt, causing an event message to be sent to the application so it can start consuming data. Once the data has been consumed, the application can post the data buffer back on the queue. This can go on indefinitely.

One of the great advantages of Async DMA is that almost 95% of CPU cycles are available for data processing, as all DMA arming is done on an event-driven basis.

To the best of our knowledge, no other supplier of waveform digitizers provides asynchronous software drivers. Their synchronous drivers force the CPU to manage data acquisition, thereby slowing down the overall data acquisition process.

Triggering

ATS9626 is equipped with sophisticated digital triggering options, such as programmable trigger thresholds and slope on any of the input channels or the External Trigger input.

Coprocessor FPGA has access to external trigger and two auxiliary I/O signals and users can create sophisticated custom trigger circuits.

The user can specify the number of records to capture in an acquisition, the length of each record and the amount of pre-trigger data.

A programmable trigger delay can also be set by the user. This is very useful for capturing the signal of interest in a pulse-echo application, such as ultrasound, radar, lidar etc.

External Trigger Input

The external trigger input on the ATS9626 is labeled TRIG IN on the face plate.

External Trigger must an LVTTL digital signal, i.e. 0 to 3.3 V TTL signal. Minimum pulse height requirement is 2.0 Volts. Input impedance of this input is 6.4 kΩ.

Analog signals and smaller amplitude digital signals will not be detected as trigger events.

User can select between rising edge and falling edge of this signal as the trigger event.

It should be noted that the TRIG IN signal passes through the Coprocessor FPGA. This description of TRIG IN applies to the default Coprocessor FPGA shipped with ATS9626 drivers. A custom Coprocessor FPGA can completely change the functionality of this signal.

Timebase

ATS9626 timebase can be controlled either by on-board low-jitter VCO or by optional External Clock.

On-board low-jitter VCO uses an on-board 10 MHz TCXO as a reference clock.

Optional External Clock

While the ATS9626 features low jitter VCO and a 10 MHz TCXO as the source of the timebase system, there may be occasions when digitizing has to be synchronized to an external clock source.

ATS9626 External Clock option provides an SMA input for an external clock signal, which can be a sine wave or 1.6V digital signal.

Input impedance for the External Clock input is fixed at 50 Ω. External clock input is always ac-coupled.

There are two types of External Clock supported by ATS9626: Fast External Clock, and 10 MHz Reference Clock.

Fast External Clock

A new sample is taken by the on-board ADCs for each rising edge of this External Clock signal.

In order to satisfy the clocking requirements of the ADC chips being used, Fast External Clock frequency must always be higher than 50 MHz and lower than 250 MHz.

This is the ideal clocking scheme for OCT applications

10 MHz Reference Clock

It is possible to generate the sampling clock based on an external 10 MHz reference input. This is useful for RF systems that use a common 10 MHz reference clock.

ATS9626 uses an on-board low-jitter VCO to generate the 250 MHz high frequency clock used by the ADC. This 250 MS/s sampled data can then be decimated by a custom Coprocessor FPGA.

Dummy Clock Switchover

OCT applications require interfacing the ATS9626 to a variable clock frequency (called k-clock) from a swept-source laser.

In most cases, k-clock frequency can be out of specification for a short period of time, i.e. the frequency is slower than 50 MHz for a short period of time.

ATS9626 has a built-in Dummy Clock generator and a clock switchover mechanism that can be used to avoid operating the A/D chips outside of their specifications.

This unique feature of the ATS9626 can be the difference between a fully working OCT system and one that cannot provide reliable data.

AUX Connectors

ATS9626 provides two AUX (Auxiliary) SMA connectors that can be used for interfacing to external digital signals.

When configured as a Trigger Output, AUX BNC connector outputs a 5 Volt TTL signal synchronous to the ATS9626 Trigger signal, allowing users to synchronize their test systems to the ATS9626 Trigger.

When combined with the Trigger Delay feature of the ATS9626, this option is ideal for ultrasonic and other pulse-echo imaging applications.

AUX connector can also be used as a Trigger Enable Input and Clock Output.

Another application for AUX connector is that users can input the 1 PPS pulse from a GPS receiver into the ATS9626 (and the Coprocessor FPGA).

Calibration

Every ATS9626 digitizer is factory calibrated to NIST-traceable standards. To recalibrate an ATS9626, the digitizer must either be shipped back to the factory or a qualified metrology lab.

AlazarDSO Software

ATS9626 is supplied with the powerful AlazarDSO software that allows the user to setup the acquisition hardware and capture, display and archive the signals.

The Stream-To-Memory command in AlazarDSO allows users to stream a large dataset to motherboard memory.

AlazarDSO software also includes powerful tools for benchmarking the computer bus and disk drive.

Software Development Kits

AlazarTech provides easy to use software development kits for customers who want to integrate the ATS9626 into their own software.

A Windows and Linux compatible software development kit, ATS-SDK, allows programs written in C/C++, C#, Python, MATLAB, and LabVIEW to fully control the ATS9626. Sample programs are provided as source code.

ATS-GPU

ATS-GPU is a software framework developed by AlazarTech to allow users to do real-time data transfer from ATS9626 to a GPU card at rates up to 1.6 GB/s.

Modern GPUs include very powerful processing units and a very high speed graphical memory bus. This combination makes them perfectly suited for signal processing applications.

ATS-GPU is supplied with an example user application in source code. The application includes GPU kernels that use ATS-GPU to receive data, do very simple signal processing (data inversion), and copy the processed (inverted) data back to a user buffer. All this is done at the highest possible data transfer rate.

Programmers can replace the data inversion code with application-specific signal processing kernels to develop custom applications.

The optional OCT Signal Processing library for ATS-GPU contains floating point FFT routines that have also been optimized to provide the maximum number of FFTs per second. Kernel code running on the GPU can do zero-padding, apply a windowing function, do a floating point FFT, calculate the amplitude and convert the result to a log scale. It is also possible to output phase information.

FFTs can be done on triggered data or on continuous gapless stream of data. It is also possible to do spectral averaging. Our benchmarks showed that it was possible to do 400,000 FFTs per second when capturing data in single-channel mode and using a NVIDIA GeForce GTX Titan X GPU.

ATS-GPU supports Windows and Linux for CUDA-based development.

Linux Support

AlazarTech offers ATS9626 binary drivers for most of the popular Linux distributions, such as CentOS, Ubuntu,...

Users can download the binary driver for their specific distribution by choosing from the available drivers here:

ftp://release@ftp.alazartech.com/outgoing/linux

Also provided is a GUI application called AlazarFrontPanel that allows simple data acquisition and display.

ATS-SDK includes source code example programs for Linux, which demonstrate how to acquire data programmatically using a C compiler.

If customers want to use ATS9626 in any Linux distribution other than the one listed above, they can have the AlazarTech engineering team generate an appropriate driver for a nominal fee.

Based on a minimum annual business commitment, the Linux driver source code license (order number ATS9626-LINUX) may be granted to qualified OEM customers for a fee. For release of driver source code, a Non-Disclosure Agreement must be executed between the customer's organization and AlazarTech.

All such source code disclosures are made on an as-is basis with limited support from the factory.

Export Control Classification

According to the latest Export Control Handbook that came into effect on August 11, 2017, ATS9626 is classified by Export Controls Division of Government of Canada as a controlled product under ECL 1-3.A.2.h, which is equivalent to ECCN 3A002.h.

For sales where the ultimate country destination is Canada or U.S., no export permit is required unless the end-use of ATS9626, in part or in its entirety, is related to the development or deployment of weapons of mass destruction.

For shipments to eligible destinations, AlazarTech is allowed to export under a general export permit, unless the end-use of ATS9626, in part or in its entirety, is related to the development or deployment of weapons of mass destruction. For general export permit shipments, users must provide a signed export compliance statement (ECS) that includes a detailed description of the end-use. Shipments cannot be made without a signed ECS on file.

For all other countries, and for all cases where the end-use of ATS9626, in part or in its entirety, is related to the development or deployment of weapons of mass destruction, an export permit is required, which will require extensive details on the end-use and end-users. This process may cause significant delays.

RoHS Compliance

ATS9626 is fully RoHS compliant, as defined by Directive 2011/65/EU (RoHS 2) of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

All manufacturing is done using RoHS-compliant components and lead-free soldering.

EC Conformity

ATS9626 conforms to the following standards:

Electromagnetic Emissions:
CISPR 22:2006/EN 55022:2006 (Class A):
Information Technology Equipment (ITE). Radio disturbance characteristics. Limits and method of measurement.

Electromagnetic Immunity:
CISPR 24:1997/EN 55024:1998 (+A1 +A2):
Information Technology Equipment Immunity characteristics — Limits and methods of measurement.

Safety:
IEC 60950-1:2005: Information technology equipment — Safety — Part 1: General requirements.

IEC 60950-1:2006: Information technology equipment — Safety — Part 1: General requirements.

ATS9626 also follows the provisions of the following directives: 2006/95/EC (Low Voltage Equipment); 2004/108/EC (Electromagnetic Compatibility).

FCC & ICES-003 Compliance

ATS9626 has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15, subpart B of the FCC Rules, and the Canadian Interference-Causing Equipment Standard ICES-003:2004.

Processing Using Multiple CPU Cores

Programmers can take advantage of multiple cores available in modern CPUs to speed up signal processing.

Benchmarks have shown that a quad-core CPU can perform real-time averaging at a rate of 1.0 GB/s and only use up 20% of CPU cycles. Increasing the number of cores or decreasing the sample rate reduces CPU usage even further.

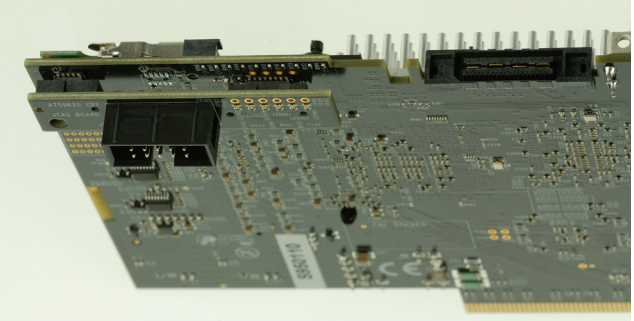
One of the main applications of using multiple cores to do signal processing is Quantum Computing and Spectroscopy applications, where each record contains partial information about the signal of interest and a large number of records must be accumulated to gather a representative dataset.

FPGA Development Kit

Customers who want to design their own Coprocessor FPGA must purchase the ATS962x Coprocessor FPGA Development Kit, which is sold separately.

This kit consists of example project provided in VHDL source code and all required project files for Quartus II software.

Also included is a JTAG Debug Board that will allow FPGA designers to debug their designs using SignalTap in-system logic analyzer and USB Blaster cable from Altera.



To further assist the user, AlazarTech will also include a very high quality 1 meter long PCI Express bus extension cable that will allow the ATS9626 to be brought out of the chassis and on to the bench, so various LEDs are visible.

Customers must have good working knowledge of FPGA development using Altera tools in order to take advantage of the ATS9626 FPGA Development Kit.

ATS9626

250 MS/s 16-Bit DC-coupled PCI Express Digitizer with user-programmable FPGA

System Requirements

Personal computer with at least one free x8 or x16 PCI Express (v1.0a, v1.1 or v2.0) slot, 2 GB RAM, 100 MB of free hard disk space, SVGA display adaptor and monitor with at least a 1024 x 768 resolution.

Power Requirements

+12 V	2.0 A, typical
+3.3 V	2.0 A, typical

Physical

Size	Single slot, half length PCI card (4.2 inches x 6.5 inches)
Weight	250 g

I/O Connectors

ECLK, CH A, CH B, TRIG IN, AUX I/O 1, AUX I/O 2	SMA female connectors

Environmental

Operating temperature	0 to 55 degrees Celsius
Storage temperature	-20 to 70 degrees Celsius
Relative humidity	5 to 95%, non-condensing

Acquisition System

Resolution	16 bits
Bandwidth (-3 dB) DC-coupled, 50 Ω	Without ATS9626-014 upgrade: DC - 120 MHz With ATS9626-014 upgrade: DC - 100 MHz
Number of channels	2, simultaneously sampled
Maximum Sample Rate	250 MS/s single shot
Minimum Sample Rate	1 KS/s single shot for internal clocking
Full Scale Input range:	±1.25 V standard. Can be permanently changed to ±200 mV with ATS9626-014 upgrade
Input coupling	DC only
Input impedance	50 Ω ±1%
Input protection	±4 V (DC + peak AC for CH A, CH B and EXT only without external attenuation)

Timebase System

Timebase options	Internal Clock or External Clock (Optional)
Internal Sample Rates	250 MS/s, 125 MS/s, 100 MS/s, 50 MS/s, 20 MS/s, 10 MS/s, 5 MS/s, 2 MS/s, 1 MS/s, 500 KS/s, 200 KS/s, 100 KS/s, 50 KS/s, 20 KS/s, 10 KS/s, 5 KS/s, 2 KS/s, 1 KS/s
Internal Clock accuracy	±2 ppm

Dynamic Parameters

Typical values measured on CH A of a randomly selected ATS9626. Input signal was provided by a Marconi 2018A signal generator, followed by multi-pole band-pass filters (TTE Q36T family). Inputs were not averaged.

	5 MHz	10 MHz	20 MHz	50 MHz	100 MHz
SNR	72.90 dB	72.32 dB	72.27 dB	71.19 dB	67.97 dB
SINAD	72.35 dB	71.97 dB	71.66 dB	65.95 dB	58.74 dB
SFDR	95.36 dB	95.10 dB	91.69 dB	90.20 dB	89.23 dB
THD	-81.58 dB	-83.06 dB	-80.93 dB	-67.50 dB	-59.28 dB
ENOB	11.73	11.66	11.62	10.66	9.46

Optional ECLK (External Clock) Input

Signal Level	200 mVp-p to 3.3 Vp-p sine wave or square wave
Input impedance	50Ω
Input coupling	AC
Maximum frequency	250 MHz for Fast External Clock
Minimum frequency	50 MHz for Fast External Clock
Sampling Edge	Rising

Dummy Clock Switchover

Switchover mode	Only when Fast External Clock is selected
Switchover start	Upon end of each record
Switchover time	Programmable with 5 ns resolution

Optional 10 MHz Reference Input

Signal Level	200 mVp-p to 3.3 Vp-p sine wave or square wave
Input impedance	50 Ω
Input Coupling	AC coupled
Input Frequency	10 MHz ± 0.25 MHz
Sampling Clock Freq.	250 MHz

Triggering System

Mode	Edge triggering with hysteresis
Comparator Type	Digital comparators for internal (CH A, CH B) triggering and analog comparators for TRIG IN (External) triggering
Number of Trigger Engines	2
Trigger Engine Combination	OR,
Trigger Engine Source	CH A, CH B, EXT, Software or None, independently software selectable for each of the two Trigger Engines
Hysteresis	±5% of full scale input, typical
Trigger sensitivity	±10% of full scale input range. This implies that the trigger system may not trigger reliably if the input has an amplitude less than ±10% of full scale input range selected
Trigger level accuracy	±5%, typical, of full scale input range of the selected trigger source

ATS9626

250 MS/s 16-Bit DC-coupled PCI Express Digitizer with user-programmable FPGA

Bandwidth	50 MHz
Trigger Delay	Software selectable from 0 to 9,999,999 sampling clock cycles
Trigger Timeout	Software selectable with a 10 µs resolution. Maximum settable value is 3,600 seconds. Can also be disabled to wait indefinitely for a trigger event

TRIG IN (External Trigger) Input

Input type	Digital triggering (LVTTL)
Input impedance	6.4 kΩ ±10%
Coupling	DC only
Minimum pulse width	16 nanoseconds
Minimum pulse amplitude	2 Volt
Absolute maximum input	-0.7 V to +8 V

TRIG OUT Output

Connector Used	AUX I/O
Output Signal	5 Volt TTL
Synchronization	Synchronized to a clock derived from the ADC sampling clock. Divide-by-4 clock (dual channel mode) or divide-by-8 clock (single channel mode)

Materials Supplied

ATS9626 PCI Express Card

ATS9626 Installation Disk (on USB Flash Drive)

Certification and Compliances

RoHS 2 (Directive 2011/65/EU) Compliance

CE Marking — EC Conformity

FCC Part 15 Class A / ICES-003 Class A Compliance

All specifications are subject to change without notice

ORDERING INFORMATION

ATS9626-2G-SL50	ATS9626-002
ATS9626-2G-SE260	ATS9626-003
SyncBoard-9626 2x	ATS9626-007
SyncBoard-9626 4x	ATS9626-008
ATS9626: High Capacity FPGA Upgrade	ATS9626-013
ATS9626: ±200mV Input Range Upgrade	ATS9626-014
SyncBoard-9626 2x-W	ATS9626-020
SyncBoard-9626 3x-W	ATS9626-021
SyncBoard-9626 4x-W	ATS9626-022
ATS9626-SL50: One Year Extended Warranty	ATS9626-061
ATS9626-SE260: One Year Extended Warranty	ATS9626-062
ATS9626: FPGA Development Kit	ATS9626-FDK
Software Development Kit (Supports C/C++, Python, MATLAB, and LabVIEW)	ATS-SDK
ATS-GPU-BASE: GPU streaming framework 1 Year Subscription	ATSGPU-001
ATS-GPU-OCT: Signal Processing Library 1 Year Subscription (requires ATSGPU-001)	ATSGPU-101

Manufactured By:

Alazar Technologies, Inc.

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DATASHEET REVISION HISTORY

Changes from version 1.3 (Mar 2017) to version 1.3A	Section, Page
Added section on External Trigger Input	External Trigger Input, pg. 5
Modified AlazarDSO description	AlazarDSO Software, pg. 6
Specified conditions for obtaining a Linux driver source code license	Linux Support, pg. 6
Replaced *ATS-GPU Compatibility* section with new *ATS-GPU* section	ATS-GPU, pg. 6
Replaced section *ATS-Linux* with *Linux Support*; now includes download link & updated description	Linux Support, pg. 7
Added Export Control Classification information	Export Control Classification, pg. 7
Added section on RoHS compliance	RoHS Compliance, pg. 7
Added section on EC Conformity	EC Conformity, pg. 7
Added section on FCC & ICES-003 Compliance	FCC & ICES-003 Compliance, pg. 7
Updated External Trigger Input Impedance to 6.4 kΩ ±10%	TRIG IN (External Trigger) Input, pg. 10
Updated list of Certification and Compliances	Certification and Compliances, pg. 10
Removed products ATS9626-LINUX, ATSGPU-BASE, ATSGPU-ANN, ATSGPU-FFT	Ordering Information System, pg. 10
Added products ATS9626-061, ATS9626-062, ATSGPU-001, ATSGPU-101	Ordering Information System, pg. 10
Corrected product name for ATS-SDK	Ordering Information, pg. 10

Changes from version 1.1C (Jan 2013) to version 1.3	Section, Page
Added Python to list of supported SDK programming languages	Features + Overview, pg. 1
Updated list of supported Operating Systems	Feature Table, pg. 1
Corrected ATS9626 Coprocessor FPGA Development Kit name & part number	Overview, pg. 1
Modified SDK description to add Python support and remove ATS-VI	Overview, pg. 1
Added analog input bandwidth specifications specific to ATS9626-014 upgrade	Analog Input, pg. 2
Added 2-slot-spacing SyncBoards (-W models)	Master/Slave Systems, pg. 5
Modified SDK description to add Python support and remove ATS-VI	Software Development Kits, pg. 6
Replaced *GPU Based Signal Processing* information with *ATS-GPU Compatibility*	ATS-GPU Compatibility, pg. 6
Added acquisition system bandwidth specifications specific to ATS9626-014 upgrade	Acquisition System, pg. 8
Added new part numbers to Ordering Information	Ordering Information, pg. 9