ATS9462 is a 4-lane PCI Express (PCIe x4), dual-channel, high resolution, 16-bit, 180 MS/s waveform digitizer card capable of streaming acquired data to PC memory at rates up to 720 MB/s.

The basic ATS9462 model uses an on-FPGA FIFO to stream data to host PC memory. ATS9462 is also available with up to 512 MegaSamples of on-board, dual port memory per channel. This memory can be used as a very deep FIFO to mitigate system latencies during sustained data transfer.

Users can capture data from one trigger or a burst of triggers. Users can also stream very large datasets continuously to PC memory or hard disk.

ATS9462 allows users to build real-time data acquisition systems even under the Windows or Linux operating systems, as users are allowed to read acquired data while the next acquisition is in progress.

ATS9462 PCI digitizers are an ideal solution for cost sensitive OEM applications that require a digitizer to be embedded into the customer’s equipment.

ATS9462 is supplied with AlazarDSO software that lets the user get started immediately without having to go through a software development process.

Users who need to integrate the ATS9462 in their own program can purchase a software development kit, ATS-SDK for C/C++ and VB, or ATS-VI for LabVIEW for Windows or a Linux based ATS-Linux.

All of this advanced functionality is packaged in a low power, half-length PCI Express card.

### Overview

**Product** | **Bus** | **Operating System** | **Channels** | **Sampling Rate** | **Bandwidth** | **Memory Per Channel** | **Resolution**
---|---|---|---|---|---|---|---
ATS9462 | PCIe x4 | Windows 2K/XP, Vista, Linux 2.6 | 2 | 180 MS/s to 1 KS/s | 65 MHz | FIFO-Only, 64M, 512M | 16 bits

### Applications

- Optical Coherence Tomography (OCT)
- Ultrasonic & Eddy Current NDT/NDE
- Radar/RF Signal Recording & Analysis
- Terabyte Storage Oscilloscope
- High Resolution Oscilloscope
- Lidar
- Spectroscopy
- Digital Down Conversion (DDC)
- Multi-Channel Transient Recording
PCI Express Bus Interface
ATS9462 interfaces to the host computer using a 4-lane PCI Express bus. Each lane operates at 2.5 Gbps. PCIe bus specification v1.0a and v1.1 are supported.

According to PCIe specification, a 4-lane board can be plugged into any 4-lane, 8-lane or 16-lane slot, but not into a 1-lane slot. As such, ATS9462 requires at least one free 4-lane, 8-lane or 16-lane slot on the motherboard.

The physical and logical PCIe x4 interface is provided by an on-board FPGA, which also integrates acquisition control functions, memory management functions and acquisition datapath. This very high degree of integration allows for optimum product reliability.

PCI Express is a relatively new bus and, as such, throughput performance may vary from motherboard to motherboard. AlazarTech’s 720 MB/s benchmarks were done using a Dell Precision 390 workstation.

Users must always be wary of throughput specifications from manufacturers of waveform digitizers. Some unscrupulous manufacturers tend to specify the raw, burst-mode throughput of the bus. AlazarTech, on the other hand, specifies the benchmarked sustained throughput. To achieve such high throughput, a great deal of proprietary memory management logic and kernel mode drivers have been designed.

Analog Input
An ATS9462 features two analog input channels with extensive functionality. Each channel has 65 MHz of full power analog input bandwidth. With software selectable attenuation, you can achieve an input voltage range of ±200mV to ±16V. Attenuating probes (sold separately) can extend the voltage range even higher.

Software selectable AC or DC coupling further increases the signal measurement capability. Software selectable 50Ω input impedance makes it easy to interface to high speed RF signals.

Amplifier Bypass Mode
To obtain optimum dynamic performance, choose the Amplifier Bypass Mode. This mode comes standard with the ATS9462.

Each channel can be independently bypassed using on-board DIP-switches.

Once the amplifier has been bypassed, the input for that channel has 50Ω impedance, DC coupling and a 550 mV full scale input range. Diode protection is still included, but users should avoid saturation of the input beyond 120% of full scale.

Wideband Input Upgrade
Some applications, such as Digital Video Broadcast (DVB), require analog input bandwidth to be higher than the standard bandwidth of ATS9462.

A Wideband Input Upgrade can be purchased for such cases. Bandwidth can be extended to 120 MHz with minimal effect on noise performance.

Acquisition System
ATS9462 PCI digitizers use a pair of state of the art 180MS/s, 16-bit ADCs to digitize the input signals. The real-time sampling rate ranges from 180 MS/s down to 1 KS/s. The two channels are guaranteed to be simultaneous, as they share the exact same clock.

An acquisition can consist of multiple records, with each record being captured as a result of one trigger event. A record can contain both pre-trigger and post-trigger data.

Infinite number of triggers can be captured by ATS9462 while operating in dual-port memory mode.

In between the multiple triggers being captured, the acquisition system is re-armed by the hardware within 32 sampling clock cycles.

This mode of capture, sometimes referred to as Multiple Record, is very useful for capturing data in applications with a very rapid or unpredictable trigger rate. Examples of such applications include medical imaging, ultrasonic testing, OCT and NMR spectroscopy.

Maximum Sustained Transfer Rate
PCI Express support on different motherboards is not always the same, resulting in significantly different sustained data transfer rates. The reasons behind these differences are complex and varied and will not be discussed here.

ATS9462 users can quickly determine the maximum sustained transfer rate for their motherboard by inserting their card in a PCIe slot and running the Tools:Benchmark:Bus tool provided in AlazarDSO software.

FIFO-Only Model
A FIFO-only model of ATS9462 is available for OEMs who need optimal cost and do not need any on-board memory.

In this mode, an on-FPGA FIFO is used to buffer ADC data. The size of the FIFO is 8 kilobytes.

FIFO-only acquisition mode can work for both single record and multiple record acquisitions. The only restrictions are that there will be limited pre-trigger acquisition, no time-stamping and no buffer headers.
It is also possible to stream a very long, gapless dataset using the on-board FIFOs.

FIFO-only acquisition mode can be used for scanning applications such as OCT, ultrasonic inspection, radar and lidar.

It should be noted that FIFO-only model may not be able to achieve the Maximum Sustained Transfer Rate of a particular motherboard, as the operating system, or another resource on the motherboard, may temporarily interrupt the DMA transfer, causing the on-FPGA FIFO to overflow.

In other words, FIFO-only data acquisition is heavily dependent on the quality of the motherboard if the bus throughput exceeds 400 MB/second.

For faster throughput, it is highly recommended that models with on-board memory be used.

**On-Board Acquisition Memory**

ATS9462 supports on-board memory buffers of 64 MegaSamples and 512 MegaSamples per channel.

There are two distinct advantages of having on-board memory:

First, a snapshot of the ADC data can be stored into this acquisition memory at full acquisition speed without any concern for the bus throughput.

Second, and more importantly, on-board memory can also act as a very deep FIFO between the Analog to Digital converters and PCI Express bus, allowing very fast sustained data transfers across the bus, even if the operating system or another motherboard resource temporarily interrupts DMA transfers.

Therefore, an ATS9462 equipped with on-board acquisition memory does achieve the Maximum Sustained Transfer Rate of a motherboard.

**Traditional AutoDMA**

In order to acquire both pre-trigger and post-trigger data in a dual-ported memory environment, users can use Traditional AutoDMA.

Data is returned to the user in buffers, where each buffer can contain from 1 to 8191 records (triggers). This number is called RecordsPerBuffer.

As shown in the diagram above, each record is transferred to PC host memory as soon as it is acquired.

Users can also specify that each record should come with its own header that contains a 40-bit trigger timestamp.

A BUFFER_OVERFLOW flag is asserted if more than 512 buffers have been acquired by the acquisition system, but not transferred to host PC memory by the AutoDMA engine.

While Traditional AutoDMA can acquire data to PC host memory at the maximum sustained transfer rate of the motherboard, a BUFFER_OVERFLOW can occur if more than 512 triggers occur in very rapid succession, even if all the on-board memory has not been used up.

**No Pre-Trigger (NPT) AutoDMA**

Many ultrasonic scanning and medical imaging applications do not need any pre-trigger data: only post-trigger data is sufficient.

NPT AutoDMA is designed specifically for these applications. By only storing post-trigger data, the memory bandwidth is optimized and the entire on-board memory acts like a very deep FIFO.

Note that a DMA is not started until RecordsPerBuffer number of records (triggers) have been acquired.

NPT AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

More importantly, a BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up. This provides a very substantial improvement over Traditional AutoDMA.

NPT AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow.

This is the recommended mode of operation for most ultrasonic scanning, OCT and medical imaging applications.

**Continuous AutoDMA**

Continuous AutoDMA is also known as the data streaming mode.

In this mode, data starts streaming across the PCI bus as soon as the ATS9462 is armed for acquisition. It is important to note that triggering is disabled in this mode.
Continuous AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

The amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Continuous AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for very long signal recording.

**Triggered Streaming AutoDMA**

Triggered Streaming AutoDMA is virtually the same as Continuous mode, except the data transfer across the bus is held off until a trigger event has been detected.

Triggered Streaming AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

As in Continuous mode, the amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Triggered Streaming AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for RF signal recording that has to be started at a specific time, e.g. based on a GPS pulse.
Optional External Clock
While the ATS9462 features low jitter, high reliability 125 MHz and 100 MHz crystal oscillators and a 10 MHz TCXO as the source of the timebase system, there may be occasions when digitizing has to be synchronized to an external clock source.

ATS9462 External Clock option provides an SMA input for an external clock signal.

The input stage of the External Clock circuit is an analog comparator that converts the incoming signal into a PECL clock signal that can be used by the on-board ADCs.

Note that the input impedance for the External Clock input is fixed at 50 Ω. Input coupling for the external clock input is user-programmable between AC and DC coupling.

Fast External Clock
If the user selects Fast External Clock mode, a new sample is taken by the on-board ADCs for each rising (or falling) edge of this External Clock signal.

In order to operate the ADC under optimal conditions, the user must set the appropriate frequency range for the external clock being supplied. The following ranges are supported:

- External Clock: 1 MHz < f_{EXT} < 180 MHz

The active edge of the external clock is software selectable between the rising or falling edge.

Slow External Clock
If the external clock frequency is less than 1 MHz, then users can select Slow External Clock.

Note that Slow External Clock signal must be a 3.3 Volt TTL signal.

In this mode, the on-board ADCs are run at a fixed 125 MS/s sample rate. Each time a rising (or falling) edge is detected on the external clock signal, one sample is stored.

Thus, there can be zero to 8 ns skew between the clock edge and the actual sampling of the signal. This skew can change from sample to sample, so this type of clock should be used only if this jitter is acceptable in your application.

10 MHz Clock Reference
It is possible to generate the sampling clock based on a 10 MHz reference input. This is useful for RF systems that use a common 10 MHz reference clock.

ATS9462 uses an on-board PLL to generate the high frequency clock. Clock frequencies in the range of 150 MHz to 180 MHz can be generated with a 1 MHz resolution.

Optional LVTTL External Clock
In some OCT applications, ATS9462 has to be externally clocked by a high speed, 3.3 Volt TTL k-clock coming from a swept-source laser. In these cases, it is recommended that customers purchase the LVTTL External Clock Upgrade.

With this upgrade, the external clock input stage is optimized for receiving a high speed, 3.3 Volt TTL input in order to guarantee reliable clocking. Input impedance is also changed from 50 Ohms to 10 KOhm.

Note that some parts of the clock circuit are disabled and customers must sign a specification waiver. Contact the factory for more information.

AUX Connector - Trigger Output
ATS9462 provides an AUX (Auxiliary) BNC connector that is configured as a Trigger Output connector upon default.

When configured as a Trigger Output, AUX BNC connector outputs a 5 Volt TTL signal synchronous to the ATS9462 Trigger signal, allowing users to synchronize their test systems to the ATS9462 Trigger.

When combined with the Trigger Delay feature of the ATS9462, this option is ideal for ultrasonic and other pulse-echo imaging applications.

AUX Connector - Trigger Enable
Another use of AUX connector is its use as a Trigger Enable Input in imaging applications.

In such applications, users must first configure AUX I/O as a Trigger Enable. A FRAME_START signal should be connected to AUX I/O and LINE_START signal to TRIG IN.

Once armed, ATS9462 will not trigger until a FRAME_START pulse has arrived. It will then accept a certain number of triggers and then wait for the next FRAME_START pulse before accepting any more triggers.

This mechanism guarantees full frame image acquisition.

Calibration
Every ATS9462 digitizer is factory calibrated to NIST-traceable standards.

To periodically recalibrate an ATS9462, the digitizer must either be shipped back to the factory or a qualified metrology lab.

Calibration Software
Customers can purchase a plug-in for AlazarDSO that allows full calibration and verification of ATS9462 using an NI GPIB card and the Fluke 5820A oscilloscope calibrator.

Other oscilloscope calibrators can be used for manual calibration.
Master/Slave Systems
Up to 8 inputs can be sampled simultaneously using multiple ATS9462 boards configured as a Master/Slave system by using a SyncBoard 9462 of appropriate width.

SyncBoard 9462 is a mezzanine board and plugs into the connector located at the top of the ATS9462 boards.

A SyncBoard 9462 uses the clock output from a Master board and delivers copies of that clock to all boards, Master as well as all the Slaves, using equal length traces. Note that no PLL is used for clock buffering, thus ensuring truly simultaneous sampling even when the clock frequency is not constant.

SyncBoard 9462 also allows any of the boards to trigger the entire Master/Slave system.

It should be noted that PCI Express is not a shared bus. As such, the data throughput is not shared between multiple boards in a Master/Slave system.

AlazarDSO Software
ATS9462 is supplied with the powerful AlazarDSO oscilloscope emulation software that allows the user to setup the acquisition hardware and capture, display and archive the signals.

AlazarDSO is available in English, French, German, Spanish, Japanese and Chinese languages.

A built-in FFT engine allows AlazarDSO to display acquired data in both time and frequency domain.

AlazarDSO also allows users to benchmark the PCI Express bus throughput on their specific computers. In addition, users can benchmark the throughput of their disk drive(s).

Optional Stream-To-Disk Software
Sold as an optional software package for AlazarDSO, the Stream-To-Disk Module allows users to stream data to a disk volume. A volume may consist of a single disk drive or multiple drives in a RAID configuration.

Users can stream a gapless dataset, such as a Digital Video Broadcast (DVB) signal, or a triggered data stream, such as a bio-medical image signal.

This data is stored as a binary data file that can be exported to MATLAB and can also be converted to various other formats.

Optional Acquire At Time Plug-In
Users can purchase an optional plug-in for AlazarDSO that allows RF signal recording in multiple, geographically separated locations to be synchronized using a GPS signal.

Optional Calibration Plug-In
A calibration plug-in can be purchased that allows users to verify and calibrate the ATS9462 in their own laboratories.

While the verification and calibration can be done manually using any oscilloscope calibrator, the process can be very tedious.

It is recommended that users have an NI GPIB card and a Fluke 5820A oscilloscope calibrator to use this plug-in to programmatically do the verification and calibration.

ATS-SDK Software Development Kit
For customers who want to integrate the ATS9462 into their own C/C++ or VB program, AlazarTech provides a Windows compatible software development kit, ATS-SDK.

ATS-SDK includes sample programs in C and VB that demonstrate how to fully control the ATS9462 in these programming environments.

These sample programs have been tested under both 32-bit and 64-bit Windows and Vista operating systems.

ATS-VI Software Development Kit
A set of high performance vi’s for LabVIEW 7.1 and higher, called ATS-VI, can also be purchased.

Example vi’s included with ATS-VI demonstrate how to integrate the ATS9462 into a LabVIEW based vi.

ATS-VI is fully compatible with LabVIEW 8.6.

ATS9462-Linux Software Development Kit
ATS9462 is fully supported under the Linux operating system. All drivers and sample programs have been tested under Fedora Core 9 (kernel 2.6).

Linux drivers are released as C source code under a Non-Disclosure Agreement. It is the user’s responsibility to compile this source code for their version of Linux.

The driver source code and C sample programs have been tested under both 32-bit and 64-bit operating systems.
System Requirements
Personal computer with at least one free x4, x8 or x16 PCI Express (v1.0a or v1.1) slot, 512 MB RAM, 100 MB of free hard disk space, SVGA display adaptor and monitor with at least a 1024 x 768 resolution.

Power Requirements
+12V 1.2 A, typical
+3.3V 1.1 A, typical

Physical
Size Single slot, half length PCI card (4.2 inches x 7.8 inches)
Weight 250 g

I/O Connectors
CH A, CH B, TRIG IN, AUX I/O BNC female connectors
ECLK SMA female connector

Environmental
Operating temperature 0 to 55 degrees Celsius
Storage temperature -20 to 70 degrees Celsius
Relative humidity 5 to 95%, non-condensing

Acquisition System
Resolution 16 bits
Bandwidth (-3dB) DC-coupled, 1MΩ DC - 65 MHz
DC-coupled, 50Ω DC - 65 MHz
AC-coupled, 1MΩ 10 Hz - 65 MHz
AC-coupled, 50Ω 100KHz - 65 MHz
Bandwidth flatness: ± 1dB
Number of channels 2, simultaneously sampled
Maximum Sample Rate 180 MS/s single shot
Minimum Sample Rate 1 KS/s single shot for internal clocking
Full Scale Input ranges
1 MΩ input impedance: ±200mV, ±400mV, ±800mV, ±2V, ±4V, ±8V, and ±16V, software selectable
50 Ω input impedance: ±200mV, ±400mV, ±800mV, ±2V, ±4V, software selectable
DC accuracy ±2% of full scale in all ranges
Input coupling AC or DC, software selectable
Input impedance 500 or 1MΩ ±1% in parallel with 50 pF ±10pF, software selectable
Input protection 1MΩ ±28V (DC + peak AC for CH A, CH B and EXT only without external attenuation)
50Ω ±4V (DC + peak AC for CH A, CH B and EXT only without external attenuation)

Dynamic Parameters
Typical values measured using a randomly selected ATS9462 with Amplifier Bypass Mode. Input was provided by a HP8656A signal generator, followed by a 9-pole, 1 MHz band-pass filter (TTE Q36T-1M-100K-50-720B). Input frequency was set at 1 MHz and output amplitude was 520 mV rms, which was approximately 95% of the full scale input.

Amplifier Bypass Mode
Standard Feature Yes
DIP Switch selectable Yes, independently for each channel
Input Range Approx. 550 mV rms
Input Coupling DC, irrespective of the input coupling setting for the channel
Input Impedance 50 Ω, irrespective of the input impedance setting for the channel
Input bandwidth (-3dB) 85 MHz

Timebase System
Timebase options Internal Clock or External Clock (Optional)
Internal Sample Rates 180 MS/s, 160 MS/s, 125 MS/s, 100 MS/s, 50 MS/s, 20 MS/s, 10 MS/s, 5 MS/s, 2 MS/s, 1 MS/s, 500 KS/s, 200 KS/s, 100KS/s, 50 KS/s, 20 KS/s, 10 KS/s, 5 KS/s, 2 KS/s, 1 KS/s
Internal Clock accuracy ±2 ppm for 180MS/s & 160MS/s ±25 ppm for 125 MS/s and lower

Optional Wideband Input
Analog Bandwidth using Amplifier Bypass Mode 120 MHz (-3 dB)

Optional ECLK (External Clock) Input
Signal Level ±200mV to ±1V sine wave
Input impedance 50Ω
Maximum frequency 180 MHz for Fast External Clock
10 MHz for Slow External Clock
Minimum frequency 1 MHz for Fast External Clock
DC for Slow External Clock
Decimation factor Software selectable from 1 to 100,000
Sampling Edge Rising or Falling, software selectable
ATS9462
180 MS/s 16-Bit PCI Express Digitizer

Optional 10 MHz Reference Input
- Signal Level: ±200mV Sine wave or 3.3V LVTTL
- Input impedance: 50Ω
- Input Coupling: AC coupled
- Input Frequency: 10 MHz ± 0.25 MHz
- Sampling Clock Freq.: 150 MHz to 180 MHz with 1 MHz resolution

Optional 3.3V TTL Clock Input
- Signal Level: 3.3V LVTTL
- Input impedance: 10 KΩ
- Input Coupling: DC coupled
- Input Frequency: 1 MHz to 180 MHz
- Specification change: 180 MS/s & 160 MS/s internal clock rates are disabled
- 10 MHz Reference is disabled
- AC coupled external clock is disabled

Triggering System
- Mode: Edge triggering with hysteresis
- Comparator Type: Digital comparators for internal (CH A, CHB) triggering and analog comparators for TRIG IN (External) triggering
- Number of Trigger Engines: 2
- Trigger Engine Combination: OR, AND, XOR, selectable
- Trigger Engine Source: CH A, CH B, EXT, Software or None, independently software selectable for each of the two Trigger Engines
- Hysteresis: ±5% of full scale input, typical
- Trigger sensitivity: ±10% of full scale input range. This implies that the trigger system may not trigger reliably if the input has an amplitude less than ±10% of full scale input range selected
- Trigger level accuracy: ±5%, typical, of full scale input range of the selected trigger source
- Bandwidth: 65 MHz
- Trigger Delay: Software selectable from 0 to 9,999,999 sampling clock cycles
- Trigger Timeout: Software selectable with a 10 us resolution. Maximum settable value is 3,600 seconds. Can also be disabled to wait indefinitely for a trigger event

TRIG IN (External Trigger) Input
- Input Impedance: 1 MΩ in parallel with 50pF ±10pF
- Bandwidth (-3dB): DC - 25 MHz
- DC-coupled: 10 Hz - 25 MHz
- Input range: ±5V or ±1V, software selectable
- DC accuracy: ±10% of full scale input

ORDERING INFORMATION
- ATS9462
- ATS9462-64M
- ATS9462-512M
- ATS9462: External Clock Upgrade
- ATS9462: Wideband Input Upgrade
- SyncBoard 9462 2X
- SyncBoard 9462 4X
- ATS9462: LVTTL External Clock Upgrade
- ATS9462: FIFO-only to 64M Upgrade
- ATS9462: FIFO-only to 512M Upgrade
- ATS9462: 64M to 512M Upgrade
- AlazarDSO: Stream-To-Disk Module
- AlazarDSO: Acquire At Time Plug-In
- AlazarDSO: Calibration Plug-In
- AlazarDSO: Plug-In Development Kit
- C/C++, VB SDK for ATS9462
- LabVIEW VI for ATS9462
- Linux Driver for ATS9462

Materials Supplied
- ATS9462 PCI Card
- ATS9462 Hardware Manual
- ATS9462 Install Disk

Certification and Compliances
- CE Compliance
- All specifications are subject to change without notice

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