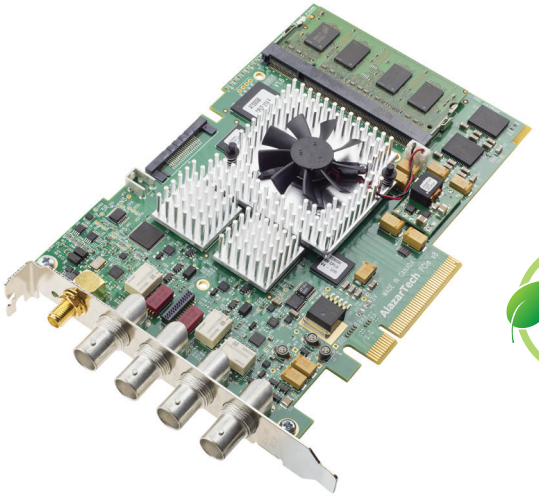
ATS9350

500 MS/s 12-Bit PCI Express Digitizer

- 1.6 GB/s PCI Express (8-lane) interface
- 2 channels sampled at 12-bit resolution
- 500 MS/s real-time sampling rate
- Variable frequency external clocking
- Up to 2 Gigasample dual-port memory
- Optional FPGA-based FFT
- ±40 mV to ±4 V input range
- Asynchronous DMA device driver
- AlazarDSO® oscilloscope software
- Software Development Kit supports C/C++, C#, Python, MATLAB®, LabVIEW®
- Support for Windows® & Linux®



RoHS 3 COMPLIANT
2015/863/EU

CE

Product	Bus	Operating System	Channels	Max. Sample Rate	Bandwidth	Memory Per Channel	Resolution
ATS9350	PCIe x8	32-bit/64-bit Windows & 64-bit Linux	2	500 MS/s	250 MHz	Up to 2 Giga-samples in single channel mode	12 bits

Overview

AlazarTech ATS®9350 is an 8-lane PCI Express (PCIe x8), dual-channel, high-speed, 12-bit, 500 MS/s waveform digitizer card capable of streaming acquired data to PC memory at rates up to 1.6 GB/s or storing it in its deep on-board dual-port acquisition memory buffer of up to 2 Gigasamples.

Up to four ATS9350 boards can be configured as a Master/Slave system to create a simultaneous sampling system of up to 8 input channels.

Unlike other products on the market, ATS9350 does not use interleaved sampling. Each input has its own 12-bit, 500 MSPS ADC chip.

Optional variable frequency external clock allows operation from 500 MHz down to 2 MHz, making ATS9350 an ideal waveform digitizer for OCT applications.

Users can capture data from one trigger or a burst of triggers. Users can also stream very large datasets continuously to PC memory or hard disk.

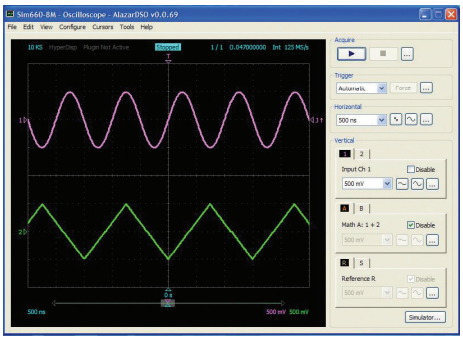
ATS9350 is supplied with AlazarDSO software that lets the user get started immediately without having to go through a software development process.

Users who need to integrate the ATS9350 in their own program can purchase a software development kit, ATS-SDK, for C/C++, C#, Python, MATLAB, and LabVIEW for both Windows and Linux operating systems.

All of this advanced functionality is packaged in a low-power, half-length PCI Express card.

Applications

Optical Coherence Tomography (OCT)
Ultrasonic & Eddy Current NDT/NDE
Radar/RF Signal Recording
Terabyte Storage Oscilloscope
High-Resolution Oscilloscope
Lidar
Spectroscopy
Multi-Channel Transient Recording



ATS9350
500 MS/s 12-Bit PCI Express Digitizer

PCI Express Bus Interface
ATS9350 interfaces to the host computer using an 8-lane PCI Express bus. Each lane operates at 2.5 Gbps. PCIe bus specification v1.0a and v1.1 are supported.

According to PCIe specification, an 8-lane board can be plugged into any 8-lane or 16-lane slot, but not into a 4-lane or 1-lane slot. As such, ATS9350 requires at least one free 8-lane or 16-lane slot on the motherboard.

The physical and logical PCIe x8 interface is provided by an on-board FPGA, which also integrates acquisition control functions, memory management functions and acquisition datapath. This very high degree of integration maximizes product reliability.

The AlazarTech® 1.6 GB/s benchmark was done on an ASUS P6T7 motherboard based on the x58 chipset for iCore processors.

Users must always be wary of throughput specifications from manufacturers of waveform digitizers. Some unscrupulous manufacturers tend to specify the raw, burst-mode throughput of the bus. AlazarTech, on the other hand, specifies the benchmarked sustained throughput. To achieve such high throughput, a great deal of proprietary memory management logic and kernel mode drivers have been designed.

Analog Input
An ATS9350 features two analog input channels with extensive functionality. Each channel has up to 250 MHz of full power analog input bandwidth. Note that the bandwidth is reduced to 150 MHz for the ±40 mV range.

With software-selectable attenuation, you can achieve an input voltage range of ±40 mV to ±4 V.

It must be noted that input impedance of both channels is fixed at 50 Ω.

Software-selectable AC or DC coupling further increases the signal measurement capability.

Acquisition System
ATS9350 PCI Express digitizers use state of the art 500 MSPS, 12-bit ADCs to digitize the input signals. The real-time sampling rate ranges from 500 MS/s down to 1 KS/s for internal clock and 2 MS/s for external clock.

The two channels are guaranteed to be simultaneous, as the two ADCs use a common clock.

An acquisition can consist of multiple records, with each record being captured as a result of one trigger event. A record can contain both pre-trigger and post-trigger data.

Infinite number of triggers can be captured by ATS9350, when it is operating using dual-port memory.

In between the multiple triggers being captured, the acquisition system is re-armed by the hardware within 256 sampling clock cycles.

This mode of capture, sometimes referred to as Multiple Record, is very useful for capturing data in applications with a very rapid or unpredictable trigger rate. Examples of such applications include medical imaging, ultrasonic testing, OCT and NMR spectroscopy.

On-Board Acquisition Memory
ATS9350 supports on-board memory buffers of 128 Megasamples, 1 Gigasamples and 2 Gigasamples.

Acquisition memory can either be divided equally between the two input channels or devoted entirely to one of the channels.

There are two distinct advantages of having on-board memory:

First, a snapshot of the ADC data can be stored into this acquisition memory at full acquisition speed of 2 ch * 500 MS/s * 2 bytes per sample = 2 Gigabytes per second, which is higher than the maximum PCIe x8 bus throughput of 1.6 GB/s.

Second, and more importantly, on-board memory can also act as a very deep FIFO between the Analog-to-Digital converters and PCI Express bus, allowing very fast sustained data transfers across the bus, even if the operating system or another motherboard resource temporarily interrupts DMA transfers.

Maximum Sustained Transfer Rate
PCI Express support on different motherboards is not always the same, resulting in significantly different sustained data transfer rates. The reasons behind these differences are complex and varied and will not be discussed here.

ATS9350 users can quickly determine the maximum sustained transfer rate for their motherboard by inserting their card in a PCIe slot and running the bus benchmarking tool provided in AlazarDSO for Windows or AlazarFrontPanel for Linux.

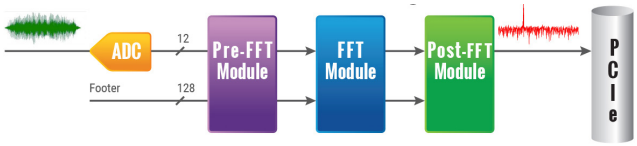
ATS9350, which is equipped with dual-port on-board memory, will be able to achieve this maximum sustained transfer rate.

Recommended Motherboards or PCs
Many different types of motherboards and PCs have been benchmarked by AlazarTech. The ones that have produced the best throughput results (as high as 1.7 GB/s for PCIe Gen 1) are listed here: www.alazartech.com/images-media/2246-AlazarTechRecommendedMotherboards.pdf.

It should be noted that some motherboards may behave unexpectedly. For example, one customer purchased a P6T6 motherboard (instead of P6T7) and found that the throughput was limited to approximately 800 MB/s because P6T6 only supports 4-lane PCI Express connection, even though it uses the same x58 chipset.

FPGA-Based FFT Processing

It is possible to do real-time FFT signal processing using the on-board FPGA. Note that only one input can be processed.



Up to 2048-point FFT length is supported. A user programmable complex windowing function can be applied to the acquired data before FFT calculation.

The complex FFT output is converted to magnitude in single precision floating-point format. A logarithmic output is also available.

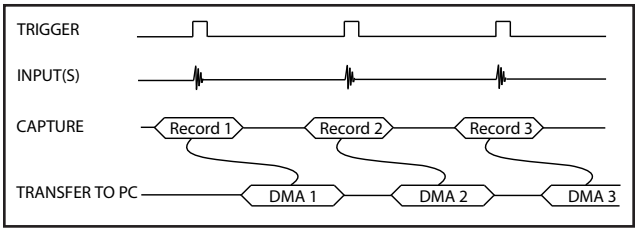
It is also possible to DMA both frequency and time domain data. This allows users to verify FPGA-based FFT operation during algorithm development.

ATS9350 can perform 100,000 2048-point FFTs per second.

FPGA-based FFT is ideal for customers in the Optical Coherence Tomography (OCT) field.

Traditional AutoDMA

In order to acquire both pre-trigger and post-trigger data in a dual-ported memory environment, users can use Traditional AutoDMA.



Data is returned to the user in buffers, where each buffer can contain from 1 to 8191 records (triggers). This number is called RecordsPerBuffer.

Users can also specify that each record should come with its own header that contains a 40-bit trigger timestamp.

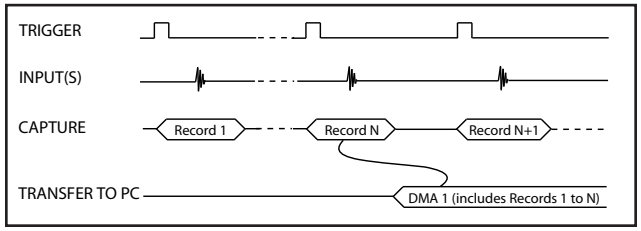
A BUFFER_OVERFLOW flag is asserted if more than 512 buffers have been acquired by the acquisition system, but not transferred to host PC memory by the AutoDMA engine.

In other words, a BUFFER_OVERFLOW can occur if more than 512 triggers occur in very rapid succession, even if all the on-board memory has not been used up.

No Pre-Trigger (NPT) AutoDMA

Many ultrasonic scanning and medical imaging applications do not need any pre-trigger data: only post-trigger data is sufficient.

NPT AutoDMA is designed specifically for these applications. By only storing post-trigger data, the memory bandwidth is optimized and the entire on-board memory acts like a very deep FIFO.



Note that a DMA is not started until RecordsPerBuffer number of records (triggers) have been acquired and written to the on-board memory.

NPT AutoDMA buffers do not include headers. However, users can specify that each record should come with its own footer that contains a 40-bit trigger timestamp. The footer is called NPT Footer.

More importantly, a BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up. This provides a very substantial improvement over Traditional AutoDMA.

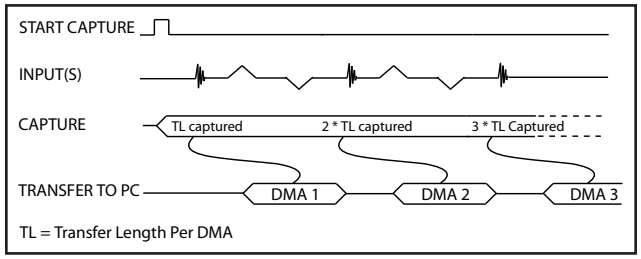
NPT AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow.

This is the recommended mode of operation for most ultrasonic scanning, OCT and medical imaging applications.

Continuous AutoDMA

Continuous AutoDMA is also known as the data streaming mode.

In this mode, data starts streaming across the PCIe bus as soon as the ATS9350 is armed for acquisition. It is important to note that triggering is disabled in this mode.



Continuous AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

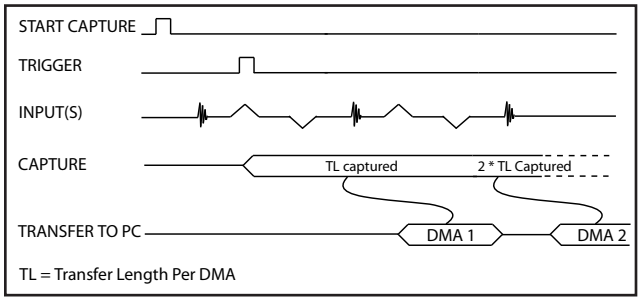
A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

The amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Continuous AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for very long signal recording.

Triggered Streaming AutoDMA

Triggered Streaming AutoDMA is virtually the same as Continuous mode, except the data transfer across the bus is held off until a trigger event has been detected.



Triggered Streaming AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

As in Continuous mode, the amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Triggered Streaming AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for RF signal recording that has to be started at a specific time, e.g. based on a GPS pulse.

Data Packing Mode

By default, ATS9350 stores 12-bit data acquired by its on-board A/D converters as a 16-bit integer. Users can also choose to pack the data as 12-bit integers or even 8-bit integers. Being able to reduce the total amount of data being transferred can be very useful in data recording applications.

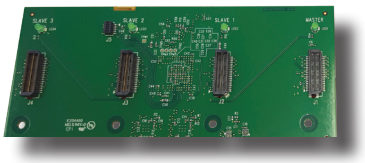
Note that it is the user application's responsibility to unpack the data.

Also note that NPT Footers are not available in Data Packing Mode.

Master/Slave Systems

Users can create a multi-board Master/Slave system by synchronizing up to four ATS9350 boards using an appropriate SyncBoard-9350. Note that ATS9350 board must be hardware version 1.3 or higher.

SyncBoard-9350 is a mezzanine board that connects to the Master/Slave connector along the top edge of the ATS9350 and sits parallel to the motherboard. For additional robustness, users can secure the SyncBoard-9350 to a bracket mounted on each of the ATS9350 boards.



SyncBoard-9350 is available in different widths: 2x, 4x, 2x-W, 3x-W or 4x-W.

SyncBoards with the -W suffix provide 2-slot spacing between ATS9350 cards to support some of the newer motherboards that space out the on-board x8 or x16 slots by two slots. The -W SyncBoards are also a better solution from thermal point of view, as there is better air flow with 2-slot spacing.

The 2x and 2x-W models allow a 2-board Master/Slave system; the 3x-W model allows a 2 or 3-slot Master/Slave system; and the 4x and 4x-W models allow 2, 3 or 4 board Master/Slave systems. The Master board's clock and trigger signals are copied by the SyncBoard-9350 and supplied to all the Slave boards. This guarantees complete synchronization between the Master board and all Slave boards.

It should be noted that SyncBoard-9350 does not use a PLL-based clock buffer, allowing the use of variable frequency clocks in Master/Slave configuration.

A Master/Slave system samples all inputs simultaneously and also triggers simultaneously on the same clock edge.

Asynchronous DMA Driver

The various AutoDMA schemes discussed above provide hardware support for optimal data transfer. However, a corresponding high-performance software mechanism is also required to make sure sustained data transfer can be achieved.

This proprietary software mechanism is called Async DMA (short for Asynchronous DMA).

A number of data buffers are posted by the application software. Once a data buffer is filled, i.e. a DMA has been completed, ATS9350 hardware generates an interrupt, causing an event message to be sent to the application so it can start consuming data. Once the data has been consumed, the application can post the data buffer back on the queue. This can go on indefinitely.

One of the great advantages of Async DMA is that almost 95% of CPU cycles are available for data processing, as all DMA arming is done on an event-driven basis.

To the best of our knowledge, no other supplier of waveform digitizers provides asynchronous software drivers. Their synchronous drivers force the CPU to manage data acquisition, thereby slowing down the overall data acquisition process.

Triggering

ATS9350 is equipped with sophisticated digital triggering options, such as programmable trigger thresholds and slope on any of the input channels or the External Trigger input.

While most oscilloscopes offer only one trigger engine, ATS9350 offers two trigger engines (called Engines J and K).

The user can specify the number of records to capture in an acquisition, the length of each record and the amount of pre-trigger data.

A programmable trigger delay can also be set by the user. This is very useful for capturing the signal of interest in a pulse-echo application, such as ultrasound, radar, lidar etc.

External Trigger Input

The external trigger input on the ATS9350 is labeled TRIG IN on the face plate.

By default, the input impedance of this input is 50 Ω and the full scale input range is +/- 3 Volts. The trigger signal is treated as an analog signal in this situation and a high-speed comparator receives the signal.

Starting with hardware version 1.5, it is also possible to trigger the ATS9350 using a 3.3 V TTL signal. Input impedance is approximately 6.3 kΩ in this mode.

Timebase

ATS9350 timebase can be controlled either by on-board low-jitter VCO or by optional External Clock.

On-board low-jitter VCO uses an on-board 10 MHz TCXO as a reference clock.

Optional External Clock

While the ATS9350 features low-jitter VCO and a 10 MHz TCXO as the source of the timebase system, there may be occasions when digitizing has to be synchronized to an external clock source.

ATS9350 External Clock option provides an SMA input for an external clock signal, which should be a high slew rate signal or LVTTL signal.

Input impedance for the External Clock input is fixed at 50 Ω. External clock input is always AC-coupled.

There are three types of External Clock supported by ATS9350. These are described below.

Fast External Clock

A new sample is taken by the on-board ADCs for each rising edge of this External Clock signal.

In order to satisfy the clocking requirements of the ADC chips being used, Fast External Clock frequency must always be higher than 2 MHz and lower than 500 MHz.

This is the ideal clocking scheme for OCT applications.

Slow External Clock

This type of clock should be used when the clock frequency is either too slow or is a burst-type clock. Both these types of clock do not satisfy the minimum clock requirements listed above for Fast External Clock.

In this mode, the ATS9350 ADCs are run at a preset internal clock frequency. The user-supplied Slow External Clock signal is then monitored for low-to-high transitions. Each time there is such a transition, a new sample is stored into the on-board memory.

It should be noted that there can be a 0 to +8 ns sampling jitter when Slow External Clock is being used, as the internal ADC clock is not synchronized to the user-supplied clock.

10 MHz Reference Clock

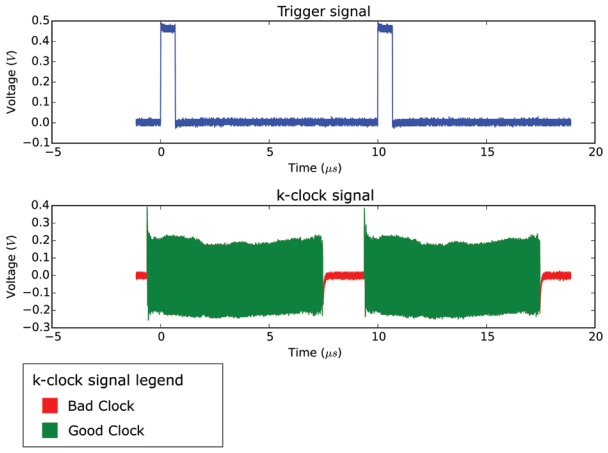
It is possible to generate the sampling clock based on an external 10 MHz reference input. This is useful for RF systems that use a common 10 MHz reference clock.

ATS9350 uses an on-board low-jitter VCO to generate the 500 MHz high-frequency clock used by the ADC. This 500 MHz sampling clock can then be decimated by a factor of 1, 2, 5, 10 or any other integer value that is divisible by 5.

OCT Ignore Bad Clock

The ADCs used on the ATS9350 require the external clock frequency to be above 2 MHz and lower than 500 MHz. In OCT applications, these limits cannot always be respected due to the nature of the optical source.

AlazarTech's *OCT Ignore Bad Clock* technology, allows safe operation with these out-of-specification clocks without requiring the use of a dummy clock in the source.



Firmware version 21.02+, driver version 5.10.6+ and SDK 7.1.3+ are required to take advantage of OCT Ignore Bad Clock. For existing customers, these firmware and driver versions are available for download from AlazarTech's website free of charge.

See www.alazartech.com/Technology/OCT-Ignore-Bad-Clock for more information on this technology.

AUX Connector

ATS9350 provides an AUX (Auxiliary) BNC connector that is configured as a Trigger Output connector by default.

When configured as a Trigger Output, AUX BNC connector outputs a 5 Volt TTL signal synchronous to the ATS9350 Trigger signal, allowing users to synchronize their test systems to the ATS9350 Trigger.

When combined with the Trigger Delay feature of the ATS9350, this option is ideal for ultrasonic and other pulse-echo imaging applications.

AUX connector can also be used as a Trigger Enable Input, or "Frame Start" input, which can be used to acquire complete frames, or B-scans, in imaging applications. In fact, this is the most popular use of the AUX connector in OCT applications.

Calibration

Every ATS9350 digitizer is factory calibrated to NIST- and CNRC-traceable standards. To recalibrate an ATS9350, the digitizer must be shipped back to the factory.

On-Board Monitoring

Adding to the reliability offered by ATS9350 are the on-board diagnostic circuits that constantly monitor over 20 different voltages, currents and temperatures. LED alarms are activated if any of the values surpass the limits.

AlazarDSO Software

ATS9350 is supplied with the powerful AlazarDSO software that allows the user to setup the acquisition hardware and capture, display and archive the signals.

The Stream-To-Memory command in AlazarDSO allows users to stream a large dataset to motherboard memory.

AlazarDSO software also includes powerful tools for benchmarking the computer bus and disk drive.

Software Development Kits

AlazarTech provides an easy-to-use software development kit for customers who want to integrate the ATS9350 into their own software.

A Windows and Linux compatible software development kit, called ATS-SDK, includes headers, libraries and source code sample programs written in C/C++, C#, Python, MATLAB, and LabVIEW. These programs can fully control the ATS9350 and acquire data in user buffers.

The purchase of an ATS-SDK license includes a subscription that provides the following benefits for a period of 12 months from the date of purchase:

- Download ATS-SDK updates from the AlazarTech website;
- Receive technical support on ATS-SDK.

Customers who want to receive technical support and download new releases beyond this 12 month period should purchase extended support and maintenance (order number ATS-SDK-1YR).

ATS-GPU

ATS-GPU is a software library developed by AlazarTech to allow users to do real-time data transfer from ATS9350 to a GPU card at rates up to 1.6 GB/s.

Modern GPUs include very powerful processing units and a very high-speed graphical memory bus. This combination makes them perfectly suited for signal processing applications.

ATS-GPU-BASE is supplied with an example user application in source code. The application includes GPU kernels that use ATS-GPU to receive data, do very simple signal processing (data inversion), and copy the processed (inverted) data back to a user buffer. All this is done at the highest possible data transfer rate.

Programmers can replace the data inversion code with application-specific signal processing kernels to develop custom applications.

ATS-GPU-OCT is the optional OCT Signal Processing library for ATS-GPU. It contains floating-point FFT routines that have also been optimized to provide the maximum number of FFTs per second. Kernel code running on the GPU can do zero-padding, apply a windowing function, do a floating-point FFT, calculate the amplitude and convert the result to a log scale. It is also possible to output phase information.

FFTs can be done on triggered data or on continuous gapless stream of data. It is also possible to do spectral averaging. Our benchmarks showed that it was possible to do 480,000 FFTs per second when capturing data in dual-channel mode and using a NVIDIA® Quadro® P5000 GPU.

ATS-GPU supports 64-bit Windows and 64-bit Linux for CUDA®-based development.

Support for Windows

Windows support for ATS9350 includes Windows 10, Windows 8.x, Windows 7 SP1 with security update KB3033929 (SHA-2 Code Signing Support), Windows Server 2012, Windows Server 2010, and Windows Server 2008 R2.

Microsoft support for Windows 7 and Windows Server 2008 R2 ends on January 14, 2020. As such, AlazarTech is ceasing development on Windows 7 and Windows Server 2008 R2 as of this date. We will continue to support customers using Windows 7 and Windows Server 2008 R2 until December 31, 2020. After this date, no support will be provided.

Due due to lack of demand and due to the fact that Microsoft no longer supports these operating systems, AlazarTech no longer supports Windows XP, Windows Vista, and Windows Server 2008.

Linux Support

AlazarTech offers ATS9350 binary drivers for the following Linux distributions: CentOS, Debian, and Ubuntu.

Users can download the binary driver for their specific distribution by choosing from the available drivers here:

ftp://release@ftp.alazartech.com/outgoing/linux

Also provided is a GUI application called AlazarFrontPanel that allows simple data acquisition and display.

ATS-SDK includes source code example programs for Linux, which demonstrate how to acquire data programmatically using a C compiler.

If customers want to use ATS9350 in any Linux distribution other than the ones listed above, they can have the AlazarTech engineering team generate an appropriate driver for a nominal fee, if applicable.

Based on a minimum annual business commitment, the Linux driver source code license (order number ATS9350-LINUX) may be granted to qualified OEM customers for a fee. For release of driver source code, a Non-Disclosure Agreement must be executed between the customer's organization and AlazarTech.

All such source code disclosures are made on an as-is basis with limited support from the factory.

Extended Warranty

The purchase of an ATS9350 includes a standard one (1) year parts and labor warranty. Customers may extend their warranty by ordering the appropriate Extended Warranty:

ATS9350-061 for ATS9350-128M
ATS9350-062 for ATS9350-1G
ATS9350-063 for ATS9350-2G

This must be purchased before expiration of the standard warranty (or before expiration of an Extended Warranty). Extended Warranties can only be purchased while there is a valid warranty in place.

AlazarTech reserves the right to limit the number of warranty extensions for any product.

Get your warranty end date by registering your product at: www.alazartech.com/UserHome?tab=2.

Export Control Classification

According to the Export Controls Division of Government of Canada, ATS9350 is currently not controlled for export from Canada. Its export control classification is N8, which is equivalent to ECCN EAR99. ATS9350 can be shipped freely outside of Canada, with the exception of countries listed on the *Area Control List* and *Sanctions List*. Furthermore, if the end-use of ATS9350, in part or in its entirety, is related to the development or deployment of weapons of mass destruction, AlazarTech is obliged to apply for an export permit.

RoHS Compliance

ATS9350 is fully RoHS compliant, as defined by Directive 2015/863/EU (RoHS 3) of the European Parliament and of the Council of 31 March 2015 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

All manufacturing is done using RoHS-compliant components and lead-free soldering.

EC Conformity

ATS9350 conforms to the following standards:

Electromagnetic Emissions:
CISPR 22:2006/EN 55022:2006 (Class A): Information Technology Equipment (ITE). Radio disturbance characteristics. Limits and method of measurement.

Electromagnetic Immunity:
CISPR 24:1997/EN 55024:1998 (+A1 +A2): Information Technology Equipment Immunity characteristics — Limits and methods of measurement.

Safety:
IEC 60950-1:2005: Information technology equipment — Safety — Part 1: General requirements.

IEC 60950-1:2006: Information technology equipment — Safety — Part 1: General requirements.

ATS9350 also follows the provisions of the following directives: 2006/95/EC (Low Voltage Equipment); 2004/108/EC (Electromagnetic Compatibility).

FCC & ICES-003 Compliance

ATS9350 has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15, subpart B of the FCC Rules, and the Canadian Interference-Causing Equipment Standard ICES-003:2004.

ATS9350

500 MS/s 12-Bit PCI Express Digitizer

System Requirements

Personal computer with at least one free x8 or x16 PCI Express (v1.0a, v1.1 or v2.0) slot, 2 GB RAM, 100 MB of free hard disk space, SVGA display adaptor and monitor with at least a 1024 x 768 resolution.

Power Requirements

+12 V	1.2 A, typical
+3.3 V	1.1 A, typical

Physical

Size	Single slot, half length PCI Express card (4.377 inches x 6.5 inches excluding the connectors protruding from the front panel)
Weight	250 g

I/O Connectors

CH A, CH B, TRIG IN, AUX I/O	BNC female connectors
ECLK	SMA female connector

Environmental

Operating temperature	0 to 55 degrees Celsius
Storage temperature	-20 to 70 degrees Celsius
Relative humidity	5 to 95%, non-condensing

Acquisition System

Resolution	12 bits
Bandwidth (-3 dB)	
DC-coupled, 50 Ω	±40 mV range: DC - 150 MHz All other ranges: DC - 250 MHz
AC-coupled, 50 Ω	±40 mV range: 100 kHz - 150 MHz All other ranges: 100 kHz - 250 MHz
Number of channels	2, simultaneously sampled
Maximum sample rate	500 MS/s single shot
Minimum sample rate	1 KS/s single shot for internal clocking
Full scale input ranges	
50 Ω input impedance:	±40 mV, ±100 mV, ±200 mV, ±400 mV, ±1 V, ±2 V, and ±4 V, software-selectable
DC accuracy	±2% of full scale in all ranges
Input coupling	AC or DC, software-selectable
Input impedance	50 Ω ±1%
Input protection	
50 Ω	±4 V (DC + peak AC for CH A, CH B, and TRIG IN only without external attenuation)

Acquisition Memory System

Memory size	128 MegaSamples, 1 GigaSamples or 2 GigaSamples
Record length	Software-selectable with 32-point resolution. Record length must be a minimum of 256 points. There is no upper limit on the maximum record length.
Number of records	Software-selectable from a minimum of 1 to a maximum of infinite number of records
Pre-trigger depth	From 0 to 4080 for single channel in NPT mode From 0 to 2040 for dual channel in NPT mode
Post-trigger depth	Record Length – Pre-Trigger Depth

Timebase System

Timebase options	Internal Clock or External Clock (Optional)
Internal sample rates	500 MS/s, 250 MS/s, 100 MS/s, 50 MS/s, 20 MS/s, 10 MS/s, 5 MS/s, 2 MS/s, 1 MS/s, 500 KS/s, 200 KS/s, 100 KS/s, 50 KS/s, 20 KS/s, 10 KS/s, 5 KS/s, 2 KS/s, 1 KS/s
Internal clock accuracy	±2 ppm

Dynamic Parameters

Typical values measured on the 400 mV range of CH A of a randomly selected ATS9350. Input signal was provided by a Rohde & Schwarz SMB100A signal generator, followed by a 9-pole, 10 MHz band-pass filter (TTE Q36T-10M-1M-50-720BMF). Input frequency was set at 9.9 MHz and output amplitude was 270 mV rms at the board's input, which is approximately 95% of the full scale input.

SNR	53.93 dB
SINAD	53.74 dB
SFDR	73.43 dB
THD	-67.61 dB
ENOB	8.63

Note that these dynamic parameters may vary from one unit to another, with input frequency and with the full scale input range selected.

Optional ECLK (External Clock) Input

Input impedance	50 Ω
Input coupling	AC
Fast External Clock	
Signal level	500 mV_{P-P} to 2 V_{P-P}
Maximum frequency	500 MHz
Minimum frequency	2 MHz
Sampling edge	Rising
Slow External Clock	
Signal Level	3.3 V LVTTL
Maximum frequency	60 MHz
Minimum frequency	DC

Optional 10 MHz Reference PLL Input

Signal level	500 mV_{P-P}
Input impedance	50 Ω
Input coupling	AC
Input frequency	10 MHz ± 0.1 MHz
Maximum frequency	10.1 MHz
Minimum frequency	9.9 MHz
Sampling clock freq.	500 MHz

ATS9350

500 MS/s 12-Bit PCI Express Digitizer

Triggering System

Mode	Edge triggering with hysteresis
Comparator type	Digital comparators for internal (CH A, CH B) triggering and software-selectable analog comparators or TTL† gate for TRIG IN (External) triggering
Number of trigger engines	2
Trigger engine combination	Engine J, engine K, J OR K, software-selectable
Trigger engine source	CH A, CH B, EXT, Software or None, independently software-selectable for each of the two Trigger Engines
Hysteresis	±5% of full scale input, typical
Trigger sensitivity	±10% of full scale input range, except for TTL† triggering for EXT. This implies that the trigger system may not trigger reliably if the input has an amplitude less than ±10% of full scale input range selected
Trigger level accuracy	±5%, typical, of full scale input range of the selected trigger source
Bandwidth	250 MHz
Trigger delay	Software-selectable from 0 to 9,999,999 sampling clock cycles
Trigger timeout	Software-selectable with a 10 µs resolution. Maximum settable value is 3,600 seconds. Can also be disabled to wait indefinitely for a trigger event

TRIG IN (External Trigger) Input

Input type	Analog or 3.3 V TTL† (5 V compliant), software-selectable
Input coupling	DC only
Analog input impedance	50 Ω
Analog bandwidth (-3 dB)	DC - 250 MHz
Analog input range	±3 V
Analog DC accuracy	±10% of full scale input
Analog input protection	±8 V (DC + peak AC without external attenuation)
TTL† input impedance	6.3 kΩ ±10%
TTL† min. pulse width	32 ADC sampling clocks
TTL† min. pulse amplitude	2 Volts
TTL† input protection	-0.7 V to +5.5 V

Auxiliary I/O (AUX I/O)

Signal direction	Input or Output, software-selectable. Trigger Output by default
Output types:	Trigger Output, Pacer (programmable clock) Output, Software-controlled Digital Output
Input types:	Trigger Enable Software readable Digital Input
Output	
Amplitude:	5 Volt TTL
Synchronization:	Synchronized to a clock derived from the ADC sampling clock. Divide-by-4 clock (dual channel mode) or divide-by-8 clock (single channel mode)
Input	
Amplitude:	3.3 Volt TTL (5 Volt compliant)

Materials Supplied

ATS9350 PCI Express card

ATS9350 Installation Disk (on USB Flash Drive)

Certification and Compliances

RoHS 3 (Directive 2015/863/EU) Compliance

CE Marking — EC Conformity

FCC Part 15 Class A / ICES-003 Class A Compliance

†*Triggering with TTL signal is available with hardware version 1.5 and higher.*

All specifications are subject to change without notice

ORDERING INFORMATION

ATS9350-128M	ATS9350-102
ATS9350-1G	ATS9350-103
ATS9350-2G	ATS9350-104
ATS9350: External Clock Upgrade	ATS9350-005
SyncBoard-9350 2x	ATS9350-006
SyncBoard-9350 4x	ATS9350-007
ATS9350-128M to 1G Upgrade	ATS9350-010
ATS9350-128M to 2G Upgrade	ATS9350-011
ATS9350-1G to 2G Upgrade	ATS9350-012
SyncBoard-9350 2x-W	ATS9350-020
SyncBoard-9350 3x-W	ATS9350-021
SyncBoard-9350 4x-W	ATS9350-022
ATS9350-128M: One Year Extended Warranty	ATS9350-061
ATS9350-1G: One Year Extended Warranty	ATS9350-062
ATS9350-2G: One Year Extended Warranty	ATS9350-063
Software Development Kit 1 Year Subscription (Supports C/C++, Python, MATLAB, and LabVIEW)	ATS-SDK
ATS-GPU-BASE: GPU Streaming Library 1 Year Subscription	ATSGPU-001
ATS-GPU-OCT: Signal Processing Library 1 Year Subscription (requires ATSGPU-001)	ATSGPU-101

Part numbers ATS9350-002, ATS9350-003 and ATS9350-004 have been discontinued and replaced respectively by ATS9350-102, ATS9350-103 and ATS9350-104, which include 2048-point FFT processing in the FPGA in addition to all the functionality of the discontinued products. New products are fully backward compatible and previously developed software will continue to work with the new products. Only the new part numbers will be shipped from here on in.

Manufactured By:

Alazar Technologies, Inc.

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DATASHEET REVISION HISTORY

Changes from version 2.0I (Jan 2020) to version 2.0J	Section, Page
Updated Dynamic Parameters. Changes are due to new testing methodology	Dynamic Parameters, pg. 8

Changes from version 2.0H (May 2019) to version 2.0I	Section, Page
Changed *Sampling Rate* column to *Max. Sample Rate*	Feature Table, pg. 1
Added AlazarFrontPanel (for Linux) as benchmarking tool	Maximum Sustained Transfer Rate, pg. 2
Replaced signal sine wave requirement with high slew rate for external clock signal	Optional External Clock, pg. 5
Removed qualified metrology lab as option for recalibrating ATS9350	Calibration, pg. 6
Specified Windows 7 version support, re-ordered list of operating systems, and added end-of-support notice for Windows 7 and Windows Server 2008 R2	Support for Windows, pg. 6
Specified Linux distributions: CentOS, Debian, and Ubuntu	Linux Support, pg. 6
Input Protection: changed External Trigger reference from "EXT" to "TRIG IN" in order to match bracket label	Acquisition System, pg. 8
Clarified specifications by separating Fast and Slow External Clock Changed fast external clock signal level from "±200 mV" to "500 mV_{P-P} to 2 V_{P-P}" Removed sine wave requirement	Optional ECLK (External Clock) Input, pg. 8
Changed signal level from ±200 mV to 500 mV_{P-P} Removed sine wave requirement and reference to slow external clock	Optional 10 MHz Reference PLL Input, pg. 8
Corrected Output types (removed Busy Output and added Pacer Output)	Auxiliary I/O (AUX I/O), pg. 9

Changes from version 2.0G (Jan 2019) to version 2.0H	Section, Page
Updated ATS-GPU benchmarks (FFTs per second, number of channels, and GPU)	ATS-GPU, pg. 6
Removed *ATS-GMA* section as this product is being discontinued	ATS-GMA, pg. 6
Added section *Extended Warranty*	Extended Warranty, pg. 7
Updated and moved Trademark information from end of document to page 7	pg. 7
Specified that listed Pre-trigger depth applies to NPT mode	Acquisition Memory System, pg. 8
Removed ATS-GMA order numbers (ATSGMA-001, ATSGMA-101)	Ordering Information, pg. 9

Changes from version 2.0F (Sept 2018) to version 2.0G	Section, Page
Updated *Sanctions List* URL	Export Control Classification, pg. 7
Updated Trademark information	pg. 9

Changes from version 2.0E (Jan 2018) to version 2.0F	Section, Page
Updated RoHS Compliance to RoHS 3	Global change
Clarified Operating System Support	Feature Table, pg. 1
Updated *Recommended Motherboards or PCs*	Recommended Motherboards or PCs, pg. 2
Correction of trigger engines: changed to J and K (instead of X and Y)	Triggering, pg. 5
Removed *Dummy Clock Switchover*, functionality replaced by *OCT Ignore Bad Clock*	Dummy Clock Switchover, pg. 6
Added information on ATS-SDK license	Software Development Kits, pg. 6
Specified 64-bit version for Windows and Linux support	ATS-GPU, pg. 6
Added *ATS-GMA* section	ATS-GMA, pg. 6
Added list of supported Microsoft Windows versions	Support for Windows, pg. 7
Removed Bandwidth Flatness	Acquisition System, pg. 8
Removed *Amplifier Bypass Mode* section	Amplifier Bypass Mode, pg. 8
Added *Acquisition Memory System* section	Acquisition Memory System, pg. 8
Added Maximum Amplitude: 2 V_{p-p}	Optional ECLK (External Clock) Input, pg. 8
Removed *Dummy Clock Switchover*, functionality replaced by *OCT Ignore Bad Clock*	Dummy Clock Switchover, pg. 8
Added "PLL" to section name for clarity, corrected Input Frequency tolerance, and added Max. and Min. Frequencies	Optional 10 MHz Reference PLL Input, pg. 8
Corrected Trigger Engine Combination	Triggering System, pg. 9

DATASHEET REVISION HISTORY

Changes from version 2.0E (Jan 2018) to version 2.0F (continued)	Section, Page
Clarified specs by providing separate specifications for Analog and TTL input, Added TTL min. pulse width, TTL min. pulse amplitude, and TTL input protection	TRIG IN (External Trigger) Input, pg. 9
Replaced *TRIG OUT Output* section with *Auxiliary I/O (AUX I/O)*	Auxiliary I/O (AUX I/O), pg. 9
Added Trademark information	pg. 9
Added subscription length for ATS-SDK, ATSGPU-001, ATSGPU-101 Added products ATSGMA-001, ATSGMA-101	Ordering Information, pg. 10

Changes from version 2.0D (Oct 2017) to version 2.0E	Section, Page
Updated and moved section on FPGA-based FFT from page 6	FPGA-based FFT Processing, pg. 3
Added note about NPT Footers	No Pre-Trigger (NPT) AutoDMA, pg. 3
Added section on Data Packing Mode	Data Packing Mode, pg. 4
Added section on OCT Ignore Bad Clock	OCT Ignore Bad Clock, pg. 5
Removed section on k-clock Deglitching Firmware	Optional k-Clock Deglitching Firmware, pg. 5
Removed note about k-clock Deglitching Firmware	Dummy Clock Switchover, pg. 5
Added CNRC as calibration standard	Calibration, pg. 5
Added note about Trigger Enable Input use in OCT	AUX Connector, pg. 6
Added -BASE and -OCT to ATS-GPU description for clarity	ATS-GPU, pg. 6
Corrected size of card	Physical, pg. 8
Removed product ATS9350-014 (k-clock Deglitching Firmware)	Ordering Information, pg. 9
Updated email address	Manufactured By, pg. 9

Changes from version 2.0C (Sept 2017) to version 2.0D	Section, Page
Updated description for product ATSGPU-001 & ATSGPU-101	Ordering Information System, pg. 9

Changes from version 2.0B (June 2017) to version 2.0C	Section, Page
Added 2-slot-spacing SyncBoards (-W models)	Master/Slave Systems, pg. 4
Specified conditions for obtaining a Linux driver source code license	Linux Support, pg. 6
Added Export Control Classification information	Export Control Classification, pg. 6
Removed product ATS9350-LINUX	Ordering Information System, pg. 9
Added products ATS9350-061, ATS9350-062, ATS9350-063	Ordering Information System, pg. 9
Replaced product ATSGPU-1YR with ATSGPU-001	Ordering Information System, pg. 9
Updated description for product ATSGPU-101	Ordering Information System, pg. 9

Changes from version 2.0A (Nov. 2013) to version 2.0B	Section, Page
Added Python to list of SDK supported languages, and Support for Windows & Linux	Features, pg. 1
Added Python & LabVIEW to list of supported languages for ATS-SDK, removed ATS-VI	Overview, pg. 1
Updated TTL Input Impedance for External Trigger	External Trigger Input, pg. 5
Modified AlazarDSO description	AlazarDSO Software, pg. 6
Updated ATS-SDK description: added Python, removed ATS-VI	Software Development Kits, pg. 6
Added ATS-GPU description	ATS-GPU, pg. 6
Replaced section *ATS-Linux* with *Linux Support* that includes download link & updated description	Linux Support, pg. 6
Added section on RoHS compliance	RoHS Compliance, pg. 6
Added section on EC Conformity	EC Conformity, pg. 7
Added section on FCC & ICES-003 Compliance	FCC & ICES-003 Compliance, pg. 7
Added TTL specification to *Comparator Type*, and *Trigger Sensitivity*	Triggering System, pg. 8
Added TTL Input Range and TTL Input Impedance for External Trigger	TRIG IN (External Trigger) Input, pg. 8
Updated list of Certification and Compliances	Certification and Compliances, pg. 8
Corrected part numbers for *SyncBoard-9350 2x, SyncBoard-9350 4x, ATS9350-LINUX*	Ordering Information, pg. 8

DATASHEET REVISION HISTORY

Changes from version 2.0A (Nov. 2013) to version 2.0B (continued)	Section, Page
Removed product ATS-VI (ATS-SDK now supports LabVIEW)	Ordering Information, pg. 8
Added products ATS9350-020, ATS9350-021, ATS9350-022, ATSGPU-1YR, ATSGPU-101	Ordering Information, pg. 8