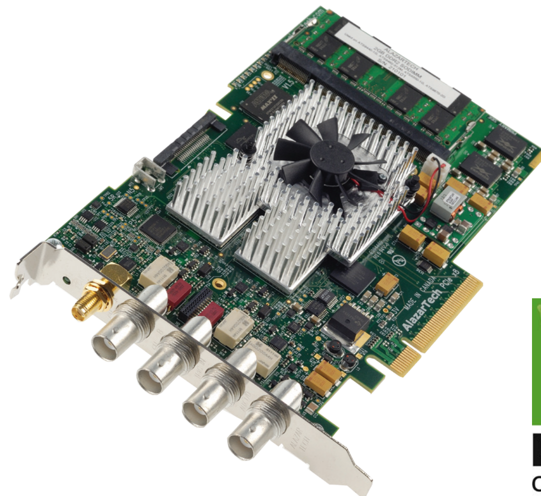
ATS9350
500MS/s 12-Bit PCI Express Digitizer

- 1.6 GB/s PCI Express (8-lane) interface
- 2 channels sampled at 12-bit resolution
- 500 MS/s real-time sampling rate
- Variable frequency external clocking
- Up to 2 GigaSample dual-port memory
- Optional FPGA-based FFT
- ±40mV to ±4V input range
- Asynchronous DMA device driver
- AlazarDSO oscilloscope software
- Software Development Kit supports C/C++, C#, MATLAB and LabVIEW
- Linux driver available



RoHS compliant
2002/95/EC

Product	Bus	Operating System	Channels	Sampling Rate	Bandwidth	Memory Per Channel	Resolution
ATS9350	PCIe x8	Win XP/Vista/7, Linux 2.6+ 32bit/64 bit	2	500 MS/s to 2 MS/s	250 MHz	Up to 2 Gig in single channel mode	12 bits

Overview

ATS9350 is an 8-lane PCI Express (PCIe x8), dual-channel, high speed, 12 bit, 500 MS/s waveform digitizer card capable of streaming acquired data to PC memory at rates up to 1.6 GB/s or storing it in its deep on-board dual-port acquisition memory buffer of up to 2 Gigasamples.

Up to four ATS9350 boards can be configured as a Master/Slave system to create a simultaneous sampling system of up to 8 input channels.

Unlike other products on the market, ATS9350 does not use interleaved sampling. Each input has its own 12-bit, 500 MSPS ADC chip.

Optional variable frequency external clock allows operation from 500 MHz down to 2 MHz, making ATS9350 an ideal waveform digitizer for OCT applications.

Users can capture data from one trigger or a burst of triggers. Users can also stream very large datasets continuously to PC memory or hard disk.

ATS9350 is supplied with AlazarDSO software that lets the user get started immediately without having to go through a software development process.

Users who need to integrate the ATS9350 in their own program can purchase a software development kit, ATS-SDK for C/C++ and MATLAB, or ATS-VI for LabVIEW for Windows or a Linux based ATS-Linux for C/C++ and LabVIEW for Linux.

All of this advanced functionality is packaged in a low power, half-length PCI Express card.

Applications

Optical Coherence Tomography (OCT)

Ultrasonic & Eddy Current NDT/NDE

Radar/RF Signal Recording

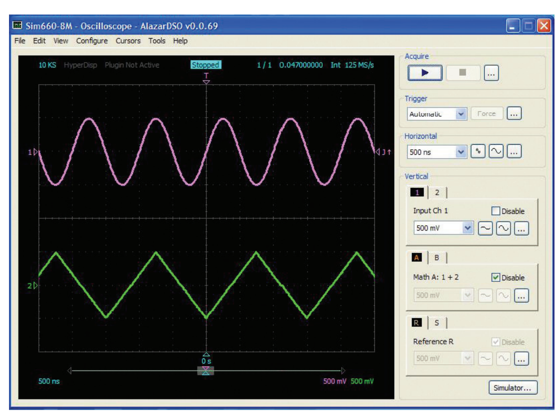
Terabyte Storage Oscilloscope

High Resolution Oscilloscope

Lidar

Spectroscopy

Multi-Channel Transient Recording



PCI Express Bus Interface

ATS9350 interfaces to the host computer using an 8-lane PCI Express bus. Each lane operates at 2.5 Gbps. PCIe bus specification v1.0a and v1.1 are supported.

According to PCIe specification, an 8-lane board can be plugged into any 8-lane or 16-lane slot, but not into a 4-lane or 1-lane slot. As such, ATS9350 requires at least one free 8-lane or 16-lane slot on the motherboard.

The physical and logical PCIe x8 interface is provided by an on-board FPGA, which also integrates acquisition control functions, memory management functions and acquisition datapath. This very high degree of integration maximizes product reliability.

PCI Express is a relatively new bus and, as such, throughput performance may vary from motherboard to motherboard. AlazarTech's 1.6 GB/s benchmark was done on an ASUS P6T7 motherboard based on the x58 chipset for iCore processors.

Other motherboards. such as Intel S5000PSL, produced similar results, whereas older machines such as the Dell T7400 also support 1.6 GB/s.

Users must always be wary of throughput specifications from manufacturers of waveform digitizers. Some unscrupulous manufacturers tend to specify the raw, burst-mode throughput of the bus. AlazarTech, on the other hand, specifies the benchmarked sustained throughput. To achieve such high throughput, a great deal of proprietary memory management logic and kernel mode drivers have been designed.

Analog Input

An ATS9350 features two analog input channels with extensive functionality. Each channel has up to 250 MHz of full power analog input bandwidth. Note that the bandwidth is reduced to 150 MHz for the ±40mV range.

With software selectable attenuation, you can achieve an input voltage range of ±40mV to ±4V.

It must be noted that input impedance of both channels is fixed at 50Ω.

Software selectable AC or DC coupling further increases the signal measurement capability.

Acquisition System

ATS9350 PCI Express digitizers use state of the art 500 MSPS, 12-bit ADCs to digitize the input signals. The real-time sampling rate ranges from 500 MS/s down to 1 KS/s for internal clock and 2 MS/s for external clock.

The two channels are guaranteed to be simultaneous, as the two ADCs use a common clock.

An acquisition can consist of multiple records, with each record being captured as a result of one trigger event. A record can contain both pre-trigger and post-trigger data.

Infinite number of triggers can be captured by ATS9350, when it is operating using dual-port memory.

In between the multiple triggers being captured, the acquisition system is re-armed by the hardware within 256 sampling clock cycles.

This mode of capture, sometimes referred to as Multiple Record, is very useful for capturing data in applications with a very rapid or unpredictable trigger rate. Examples of such applications include medical imaging, ultrasonic testing, OCT and NMR spectroscopy.

On-Board Acquisition Memory

ATS9350 supports on-board memory buffers of 128 Megasamples, 1 Gigasamples and 2 Gigasamples.

Acquisition memory can either be divided equally between the two input channels or devoted entirely to one of the channels.

There are two distinct advantages of having on-board memory:

First, a snapshot of the ADC data can be stored into this acquisition memory at full acquisition speed of 2 ch * 500 MS/s * 2 bytes per sample = 2 Gigabytes per second, which is higher than the maximum PCIe x8 bus throughput of 1.6 GB/s.

Second, and more importantly, on-board memory can also act as a very deep FIFO between the Analog to Digital converters and PCI Express bus, allowing very fast sustained data transfers across the bus, even if the operating system or another motherboard resource temporarily interrupts DMA transfers.

Maximum Sustained Transfer Rate

PCI Express support on different motherboards is not always the same, resulting in significantly different sustained data transfer rates. The reasons behind these differences are complex and varied and will not be discussed here.

ATS9350 users can quickly determine the maximum sustained transfer rate for their motherboard by inserting their card in a PCIe slot and running the Tools:Benchmark:Bus tool provided in AlazarDSO software.

ATS9350, which is equipped with dual-port on-board memory, will be able to achieve this maximum sustained transfer rate.

Recommended Motherboards

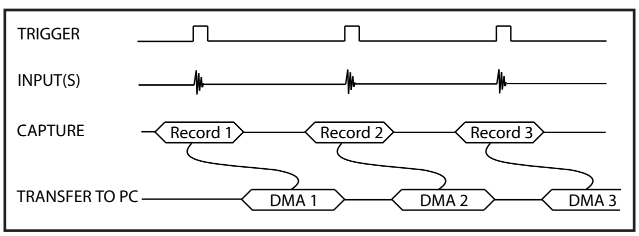
Many different types of motherboards have been benchmarked by AlazarTech. The best performance is provided by motherboards that use the Intel x58 chipset and iCore 7 processors. The motherboard that has consistently given the best throughput results (as high as 1.7 GB/s) has been te ASUS P6T7.

Older motherboards, such as Intel S5000PSLSATA that use the S5000 chipset have also provided very good (1.6 GB/s) throughput.

It should be noted that some motherboards may behave unexpectedly. For example, one customer purchased a P6T6 motherboard (instead of P6T7) and found that the throughput was limited to approximately 800 MB/s because P6T6 only supports 4-lane PCI Express connection, even though it uses the same x58 chipset.

Traditional AutoDMA

In order to acquire both pre-trigger and post-trigger data in a dual-ported memory environment, users can use Traditional AutoDMA.



Data is returned to the user in buffers, where each buffer can contain from 1 to 8191 records (triggers). This number is called RecordsPerBuffer.

Users can also specify that each record should come with its own header that contains a 40-bit trigger timestamp.

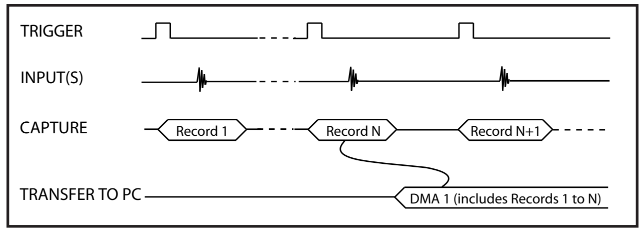
A BUFFER_OVERFLOW flag is asserted if more than 512 buffers have been acquired by the acquisition system, but not transferred to host PC memory by the AutoDMA engine.

In other words, a BUFFER_OVERFLOW can occur if more than 512 triggers occur in very rapid succession, even if all the on-board memory has not been used up.

No Pre-Trigger (NPT) AutoDMA

Many ultrasonic scanning and medical imaging applications do not need any pre-trigger data: only post-trigger data is sufficient.

NPT AutoDMA is designed specifically for these applications. By only storing post-trigger data, the memory bandwidth is optimized and the entire on-board memory acts like a very deep FIFO.



Note that a DMA is not started until RecordsPerBuffer number of records (triggers) have been acquired and written to the on-board memory.

NPT AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

More importantly, a BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up. This provides a very substantial improvement over Traditional AutoDMA.

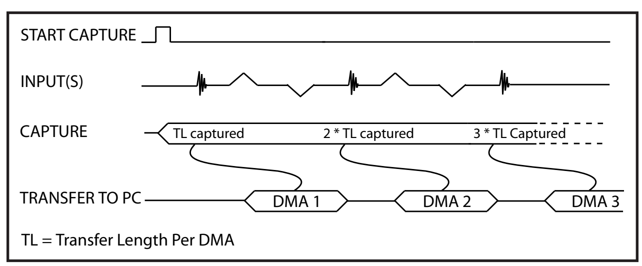
NPT AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow.

This is the recommended mode of operation for most ultrasonic scanning, OCT and medical imaging applications.

Continuous AutoDMA

Continuous AutoDMA is also known as the data streaming mode.

In this mode, data starts streaming across the PCI bus as soon as the ATS9350 is armed for acquisition. It is important to note that triggering is disabled in this mode.



Continuous AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

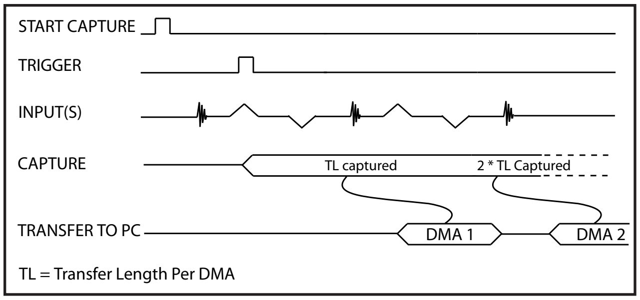
A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

The amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Continuous AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for very long signal recording.

Triggered Streaming AutoDMA

Triggered Streaming AutoDMA is virtually the same as Continuous mode, except the data transfer across the bus is held off until a trigger event has been detected.



Triggered Streaming AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

As in Continuous mode, the amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

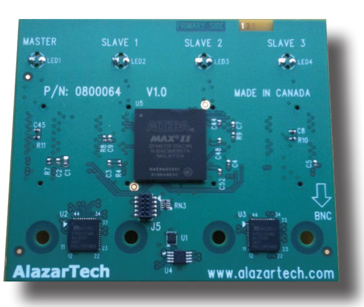
Triggered Streaming AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for RF signal recording that has to be started at a specific time, e.g. based on a GPS pulse.

Master/Slave Systems

Users can create a multi-board Master/Slave system by synchronizing up to four ATS9350 boards using an appropriate SyncBoard-9350. Note that ATS9350 board must be hardware version 1.3 or higher.

SyncBoard-9350 is available as a 2x or a 4x model: the 2x model allows a 2-board Master/Slave system whereas the 4x model allows 2, 3 or 4 board Master/Slave systems.

SyncBoard-9350 is a mezzanine board that connects to the Master/Slave connector along the top edge of the ATS9350 and sits parallel to the motherboard. For additional robustness, users can secure the SyncBoard-9350 to a bracket mounted on each of the ATS9350 boards.



The Master board's clock and trigger signals are copied by the SyncBoard-9350 and supplied to all the Slave boards. This guarantees complete synchronization between the Master board and all Slave boards.

It should be noted that SyncBoard-9350 does not use a PLL-based clock buffer, allowing the use of variable frequency clocks in Master/Slave configuration.

A Master/Slave system samples all inputs simultaneously and also triggers simultaneously on the same clock edge.

Asynchronous DMA Driver

The various AutoDMA schemes discussed above provide hardware support for optimal data transfer. However, a corresponding high performance software mechanism is also required to make sure sustained data transfer can be achieved.

This proprietary software mechanism is called Async DMA (short for Asynchronous DMA).

A number of data buffers are posted by the application software. Once a data buffer is filled, i.e. a DMA has been completed, ATS9350 hardware generates an interrupt, causing an event message to be sent to the application so it can start consuming data. Once the data has been consumed, the application can post the data buffer back on the queue. This can go on indefinitely.

One of the great advantages of Async DMA is that almost 95% of CPU cycles are available for data processing, as all DMA arming is done on an event-driven basis.

To the best of our knowledge, no other supplier of waveform digitizers provides asynchronous software drivers. Their synchronous drivers force the CPU to manage data acquisition, thereby slowing down the overall data acquisition process.

Triggering

ATS9350 is equipped with sophisticated digital triggering options, such as programmable trigger thresholds and slope on any of the input channels or the External Trigger input.

While most oscilloscopes offer only one trigger engine, ATS9350 offers two trigger engines (called Engines X and Y).

The user can specify the number of records to capture in an acquisition, the length of each record and the amount of pre-trigger data.

A programmable trigger delay can also be set by the user. This is very useful for capturing the signal of interest in a pulse-echo application, such as ultrasound, radar, lidar etc.

External Trigger Input

The external trigger input on the ATS9350 is labeled TRIG IN on the face plate.

By default, the input impedance of this input is 50Ω and the full scale input range is +/- 3 Volts. The trigger signal is treated as an analog signal in this situation and a high speed comparator receives the signal.

Starting with hardware version 1.5, it is also possible to trigger the ATS9350 using a TTL signal. Input impedance is apprixametly 2 KΩ in this mode.

Timebase

ATS9350 timebase can be controlled either by on-board low-jitter VCO or by optional External Clock.

On-board low-jitter VCO uses an on-board 10 MHz TCXO as a reference clock.

Optional External Clock

While the ATS9350 features low jitter VCO and a 10 MHz TCXO as the source of the timebase system, there may be occasions when digitizing has to be synchronized to an external clock source.

ATS9350 External Clock option provides an SMA input for an external clock signal, which can be a sine wave or LVTTL signal.

Input impedance for the External Clock input is fixed at 50 Ω. External clock input is always ac-coupled.

There are three types of External Clock supported by ATS9350. These are described below.

Fast External Clock

A new sample is taken by the on-board ADCs for each rising edge of this External Clock signal.

In order to satisfy the clocking requirements of the ADC chips being used, Fast External Clock frequency must always be higher than 2 MHz and lower than 500 MHz.

This is the ideal clocking scheme for OCT applications

Slow External Clock

This type of clock should be used when the clock frequency is either too slow or is a burst-type clock. Both these types of clock do not satisfy the minimum clock requirements listed above for Fast External Clock.

In this mode, the ATS9350 ADCs are run at a preset internal clock frequency. The user-supplied Slow External Clock signal is then monitored for low-to-high transitions. Each time there is such a transition, a new sample is stored into the on-board memory.

It should be noted that there can be a 0 to +8 ns sampling jitter when Slow External Clock is being used, as the internal ADC clock is not synchronized to the user-supplied clock.

10 MHz Reference Clock

It is possible to generate the sampling clock based on an external 10 MHz reference input. This is useful for RF systems that use a common 10 MHz reference clock.

ATS9350 uses an on-board low-jitter VCO to generate the 500 MHz high frequency clock used by the ADC. This 500 MHz sampling clock can then be decimated by a factor of 1, 2, 5, 10 or any other integer value that is divisible by 5.

Optional k-Clock Deglitching Firmware

OCT applications require interfacing the ATS9350 to a variable clock frequency (called k-clock) from a swept-source laser.

In some cases, k-clock output from the laser can contain very narrow glitches that do not satisfy FPGA timing and can cause ATS9350 to occasionally mis-trigger.

After many man-years of testing and verification with various lasers, AlazarTech has developed a special firmware for ATS9350 that limits the k-clock signal to a very small portion of the FPGA fabric, thereby eliminating mis-triggering caused by k-clock glitches.

This firmware upgrade is absolutely essential if you are using Axsun 1320nm lasers running at 50 KHz or lower. Many other lasers can also benefit from this firmare upgrade.

Dummy Clock Switchover

ATS9350 has a built-in Dummy Clock generator and a clock switchover mechanism that can be used to avoid operating the A/D chips outside of their specifications when being clocked by a wept source laser.

However, with the advent of k-clock deglitching firmware (see above), most customers have found that they do not need to use Dummy Clock.

AUX Connector

ATS9350 provides an AUX (Auxiliary) BNC connector that is configured as a Trigger Output connector by default.

When configured as a Trigger Output, AUX BNC connector outputs a 5 Volt TTL signal synchronous to the ATS9350 Trigger signal, allowing users to synchronize their test systems to the ATS9350 Trigger.

When combined with the Trigger Delay feature of the ATS9350, this option is ideal for ultrasonic and other pulse-echo imaging applications.

AUX connector can also be used as a Trigger Enable Input, or "Frame Start" input, which can be used to acquire complete frames, or B-scans, in scanning applications.

Calibration
Every ATS9350 digitizer is factory calibrated to NIST-traceable standards. To recalibrate an ATS9350, the digitizer must either be shipped back to the factory or a qualified metrology lab.

On-Board Monitoring
Adding to the reliability offered by ATS9350 are the on-board diagnostic circuits that constantly monitor over 20 different voltages, currents and temperatures. LED alarms are activated if any of the values surpasses the limits.

AlazarDSO Software
ATS9350 is supplied with the powerful AlazarDSO software that allows the user to setup the acquisition hardware and capture, display and archive the signals.

An optional Stream-To-Disk add-on module for AlazarDSO allows users to stream data to hard disk. For the fastest possible streaming, the hard disks have to be used in a RAID 0 configuration.

Users are also able to write their own Plug-In modules. A Plug-In is a DLL that is called each time AlazarDSO receives a data buffer. Many different data processing and control functions can be built into a Plug-In. Examples include Averaging, Co-Adding, controlling acquisition based on an external GPS module etc.

AlazarDSO software also includes powerful tools for benchmarking the computer bus and disk drive.

Software Development Kits
AlazarTech provides easy to use software development kits for customers who want to integrate the ATS9350 into their own software.

A Windows compatible software development kit, ATS-SDK is also offered. It allows programs written in C/C++ and MATLAB to fully control the ATS9350. Sample programs are provided as source code.

A set of high performance VIs for LabVIEW 8.6 and higher, called ATS-VI, can also be purchased.

ATS-Linux
AlazarTech offers ATS9350 binary drivers for CentOS 6.3 x86_64 with kernel 2.6.32-279.5.2.el6.x86_64. These drivers are also 100% compatible with RHEL 6.3.

Also provided is a GUI application called AlazarFrontPanel that allows simple data acquisition and display.

Source code example programs are also provided, which demonstrate how to acquire data programmatically using a C compiler.

If customers want to use ATS9350 in any Linux distribution other than the one listed above, they must purchase a license for Linux driver source code and compile the driver on the target operating system. A Non-Disclosure Agreement must also be executed between the customer's organization and AlazarTech.

All such source code disclosures are made on an as-is basis with limited support from the factory.

FPGA-based FFT
For customers in the Optical Coherence Tomography (OCT) field, a new FPGA firmware is available that allows up to 2048 point FFTs to be calculated on the acquired data on one input channel.

Only amplitude output is available. Phase output is not available at this time.

Output data can either be in 16-bit unsigned integer format or floating point format. If floating point format is selected, then it is also possible to select between normal data and logarithmic data.

A Hanning windowing function is applied prior to FFT. Future releases of this firmware may allow other windowing functions to be applied on a user-selectable basis.

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System Requirements

Personal computer with at least one free x8 or x16 PCI Express (v1.0a, v1.1 or v2.0) slot, 2 GB RAM, 100 MB of free hard disk space, SVGA display adaptor and monitor with at least a 1024 x 768 resolution.

Power Requirements

+12V	1.2 A, typical
+3.3V	1.1 A, typical

Physical

Size	Single slot, half length PCI card (4.2 inches x 6.5 inches)
Weight	250 g

I/O Connectors

CH A, CH B, TRIG IN, AUX I/O	BNC female connectors
ECLK	SMA female connector

Environmental

Operating temperature	0 to 55 degrees Celcius
Storage temperature	-20 to 70 degrees Celcius
Relative humidity	5 to 95%, non-condensing

Acquisition System

Resolution	12 bits
Bandwidth (-3dB)	
DC-coupled, 50Ω	DC - 250 MHz, typical for all input ranges other than ±40mV DC - 150 MHz, typical for ±40mV input range
AC-coupled, 50Ω	100KHz - 250 MHz, typical for all input ranges other than ±40mV 100KHz - 150 MHz, typical for ±40mV input range
Bandwidth flatness:	± 1dB to 50 MHz
Number of channels	2, simultaneously sampled
Maximum Sample Rate	500 MS/s single shot
Minimum Sample Rate	1 KS/s single shot for internal clocking
Full Scale Input ranges	
50 Ω input impedance:	±40mV, ±100mV, ±200mV, ±400mV, ±1V, ±2V, and ±4V, software selectable
DC accuracy	±2% of full scale in all ranges
Input coupling	AC or DC, software selectable
Input impedance	50Ω ±1%
Input protection	
50Ω	±4V (DC + peak AC for CH A, CH B and EXT only without external attenuation)

Amplifier Bypass Mode

Standard Feature	No
Software selectable	No. Resistor selectable. A bypass cable also must be used
Input Range	Approx. ± 200 mV
Input Coupling	DC, irrespective of the input coupling setting for the channel
Input Impedance	50 Ω, irrespective of the input impedance setting for the channel
Input bandwidth (-3dB)	250 MHz

Timebase System

Timebase options	Internal Clock or External Clock (Optional)
Internal Sample Rates	500 MS/s, 250 MS/s, 100 MS/s, 50 MS/s, 20 MS/s, 10 MS/s, 5 MS/s, 2 MS/s, 1 MS/s, 500 KS/s, 200 KS/s, 100KS/s, 50 KS/s, 20 KS/s, 10 KS/s, 5 KS/s, 2 KS/s, 1 KS/s
Internal Clock accuracy	±2 ppm

Dynamic Parameters

Typical values measured on the 200 mV range of CH A of a randomly selected ATS9350. Input signal was provided by a Marconi 2018A signal generator, followed by a 9-pole, 10 MHz band-pass filter (TTE Q36T-10M-1M-50-720BMF). Input frequency was set at 9.9 MHz and output amplitude was 135 mV rms, which was approximately 95% of the full scale input. Input was averaged.

SNR	60.55 dB
SINAD	58.09 dB
THD	-64.8 dB
SFDR	-63.05 dB

Note that these dynamic parameters may vary from one unit to another, with input frequency and with the full scale input range selected.

Optional ECLK (External Clock) Input

Signal Level	±200mV Sine wave or 3.3V LVTTL (LVTTL for Slow External Clock only)
Input impedance	50Ω
Input coupling	AC
Maximum frequency	500 MHz for Fast External Clock 60 MHz for Slow External Clock
Minimum frequency	2 MHz for Fast External Clock DC for Slow External Clock
Sampling Edge	Rising

Dummy Clock Switchover

Switchover mode	Only when Fast External Clock is selected
Switchover start	Upon end of each record
Switchover time	Programmable with 5 ns resoluton

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Optional 10 MHz Reference Input

Signal Level	±200mV Sine wave or 3.3V LVTTL (LVTTL for Slow External Clock only)
Input impedance	50Ω
Input Coupling	AC coupled
Input Frequency	10 MHz ± 0.25 MHz
Sampling Clock Freq.	500 MHz

Triggering System

Mode	Edge triggering with hysteresis
Comparator Type	Digital comparators for internal (CH A, CHB) triggering and analog comparators for TRIG IN (External) triggering
Number of Trigger Engines	2
Trigger Engine Combination	OR, AND, XOR, selectable
Trigger Engine Source	CH A, CH B, EXT, Software or None, independently software selectable for each of the two Trigger Engines
Hysteresis	±5% of full scale input, typical
Trigger sensitivity	±10% of full scale input range. This implies that the trigger system may not trigger reliably if the input has an amplitude less than ±10% of full scale input range selected
Trigger level accuracy	±5%, typical, of full scale input range of the selected trigger source
Bandwidth	250 MHz
Trigger Delay	Software selectable from 0 to 9,999,999 sampling clock cycles
Trigger Timeout	Software selectable with a 10 us resolution. Maximum settable value is 3,600 seconds. Can also be disabled to wait indefinitely for a trigger event

TRIG IN (External Trigger) Input

Input impedance	50 Ω
Coupling	DC only
Bandwidth (-3dB)	DC - 250 MHz
Input range	±3 V
DC accuracy	±10% of full scale input
Input protection	±8V (DC + peak AC without external attenuation)

TRIG OUT Output

Connector Used	AUX I/O
Output Signal	5 Volt TTL
Synchronization	Synchronized to a clock derived from the ADC sampling clock. Divide-by-4 clock (dual channel mode) or divide-by-8 clock (single channel mode)

Materials Supplied

ATS9350 PCI Express Card

ATS9350 Installation Disk (on USB Flash Drive)

Certification and Compliances

CE Compliance

All specifications are subject to change without notice

ORDERING INFORMATION

ATS9350-128M	ATS9350-102
ATS9350-1G	ATS9350-103
ATS9350-2G	ATS9350-104
ATS9350: External Clock Upgrade	ATS9350-005
SyncBoard-9350 2x	ATS9350-007
SyncBoard-9350 4x	ATS9350-008
ATS9350-128M to 1G Upgrade	ATS9350-010
ATS9350-128M to 2G Upgrade	ATS9350-011
ATS9350-1G to 2G Upgrade	ATS9350-012
ATS9350 k-clock Deglitching Firmware	ATS9350-014
C/C++, VB SDK for ATS9350	ATS-SDK
LabVIEW VI for ATS9350	ATS-VI
Linux Driver for ATS9350	ATS9350-LIN

ATS9350-002, ATS9350-003 and ATS9350-004 part numbers have been discontinued and replaced by ATS9350-102, ATS9350-103 and ATS9350-104, which include 2048 point FFT processing in the FPGA in addition to all the functionality of the discontinued products. New products are fully backward compatible and previously developed software will continue to work with the new products. Only the new part numbers will be shipped from here on in

Manufactured By:

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