ATS9352

500 MS/s 12-Bit PCI Express Digitizer

- 1.6 GB/s PCIe Gen 2 (4-lane) interface
- 2 channels sampled at 12-bit resolution
- 500 MS/s real-time sampling rate
- Variable frequency external clocking
- 128 Megasamples of on-board acquisition memory per channel
- ±100 mV to ±4 V input range
- Asynchronous DMA device driver
- AlazarDSO® oscilloscope software
- Software Development Kit supports C/C++, C#, Python, MATLAB®, LabVIEW®
- Support for Windows® & Linux®

RoHS 3 COMPLIANT
2015/863/EU

CE

Product	Bus	Operating System	Channels	Max. Sample Rate	Bandwidth	Memory Per Channel	Resolution
ATS9352	PCIe x4 Gen 2	32-bit/64-bit Windows & 64-bit Linux	2	500 MS/s	250 MHz	128 Megasamples	12 bits

Overview

AlazarTech ATS®9352 is 4-lane PCI Express Gen 2 (PCIe x4), dual-channel, high-speed, 12-bit, 500 MS/s waveform digitizer card capable of streaming acquired data to PC memory at rates up to 1.6 GB/s or storing it in its on-board dual-port acquisition memory buffer of 128 Megasamples.

Unlike other products on the market, ATS9352 does not use interleaved sampling. Each input has its own 12-bit, 500 MSPS ADC chip.

The variable frequency external clock allows operation from 500 MHz down to 25 MHz, making ATS9352 an ideal waveform digitizer for OCT applications.

Users can capture data from one trigger or a burst of triggers. Users can also stream very large datasets continuously to PC memory or hard disk.

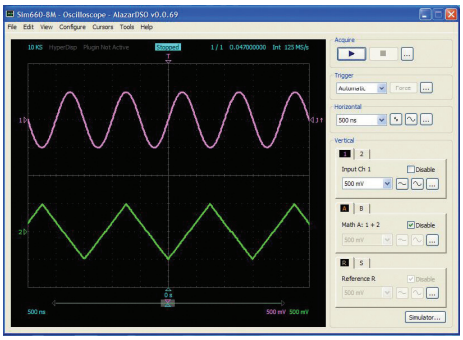
ATS9352 is supplied with AlazarDSO software that lets the user get started immediately without having to go through a software development process.

Users who need to integrate the ATS9352 in their own program can purchase a software development kit, ATS-SDK, for C/C++, C#, Python, MATLAB, and LabVIEW for both Windows and Linux operating systems.

All of this advanced functionality is packaged in a low-power, half-length PCI Express card.

Applications

Optical Coherence Tomography (OCT)
Ultrasonic & Eddy Current NDT/NDE
Radar/RF Signal Recording
Terabyte Storage Oscilloscope
High-Resolution Oscilloscope
Lidar
Spectroscopy
Multi-Channel Transient Recording



ATS9352
500 MS/s 12-Bit PCI Express Digitizer

PCI Express Bus Interface
ATS9352 interfaces to the host computer using a 4-lane PCI Express bus. Each lane operates at 5 Gbps (Gen 2).

According to PCIe specification, a 4-lane board can be plugged into any 4-lane, 8-lane or 16-lane slot, but not into a 1-lane slot. As such, ATS9352 requires at least one free 4-lane, 8-lane, or 16-lane slot on the motherboard.

Electrically, ATS9352 is compatible with Gen 2 and Gen 3 slots.

The physical and logical PCIe x4 interface is provided by an on-board FPGA, which also integrates acquisition control functions, memory management functions and acquisition datapath. This very high degree of integration maximizes product reliability.

The AlazarTech® 1.6 GB/s benchmark was done using an Asus X299-A motherboard.

The same performance can be expected from virtually all other motherboards.

Users must always be wary of throughput specifications from manufacturers of waveform digitizers. Some unscrupulous manufacturers tend to specify the raw, burst-mode throughput of the bus. AlazarTech, on the other hand, specifies the benchmarked sustained throughput. To achieve such high throughput, a great deal of proprietary memory management logic and kernel mode drivers have been designed.

Analog Input
An ATS9352 features two analog input channels with extensive functionality. Each channel has up to 250 MHz of full power analog input bandwidth.

With software-selectable attenuation, you can achieve an input voltage range of ±100 mV to ±4 V.

It must be noted that input impedance of both channels is fixed at 50 Ω.

Software-selectable AC or DC coupling further increases the signal measurement capability.

Additional Low-Frequency Analog Input
ATS9352 also features a third analog input channel capable of sampling at 200 KS/s. It allows users to acquire the value of an analog input signal each time the waveform digitizer is triggered.

The main application for this low-frequency analog input is in OCT systems where tracking or feedback signals need to be monitored in real time.

The acquired value of the third analog input is embedded into a Footer that is appended at the end of each record, so software can easily correlate all three channels.

The low-frequency analog input on the ATS9352 is labeled AN IN on the face plate.

Acquisition System
ATS9352 PCI Express digitizers use state of the art 500 MSPS, 12-bit ADCs to digitize the input signals. The real-time sampling rate ranges from 500 MS/s down to 1 KS/s for internal clock and 2 MS/s for external clock.

The two channels are guaranteed to be simultaneous, as the two ADCs use a common clock.

An acquisition can consist of multiple records, with each record being captured as a result of one trigger event. A record can contain both pre-trigger and post-trigger data.

Infinite number of triggers can be captured by ATS9352, when it is operating using dual-port memory.

In between the multiple triggers being captured, the acquisition system is re-armed by the hardware within 256 sampling clock cycles.

This mode of capture, sometimes referred to as Multiple Record, is very useful for capturing data in applications with a very rapid or unpredictable trigger rate. Examples of such applications include medical imaging, ultrasonic testing, OCT and NMR spectroscopy.

On-Board Acquisition Memory
ATS9352 provides 128 Million samples per channel of on-board dual-port memory that can be used for signal storage.

There are two distinct advantages of having on-board memory:

First, a snapshot of the ADC data can be stored into this acquisition memory at full acquisition speed of 2 ch * 500 MS/s * 2 bytes per sample = 2 Gigabytes per second, which is higher than the maximum PCIe Gen 2 x4 bus throughput of 1.6 GB/s.

Second, and more importantly, on-board memory can also act as a very deep FIFO between the Analog-to-Digital converters and PCI Express bus, allowing very fast sustained data transfers across the bus, even if the operating system or another motherboard resource temporarily interrupts DMA transfers.

Maximum Sustained Transfer Rate
PCI Express support on different motherboards is not always the same, resulting in significantly different sustained data transfer rates. The reasons behind these differences are complex and varied and will not be discussed here.

ATS9352 users can quickly determine the maximum sustained transfer rate for their motherboard by inserting their card in a PCIe slot and running the bus benchmarking tool provided in AlazarDSO for Windows or AlazarFrontPanel for Linux.

ATS9352, which is equipped with dual-port on-board memory, will be able to achieve this maximum sustained transfer rate.

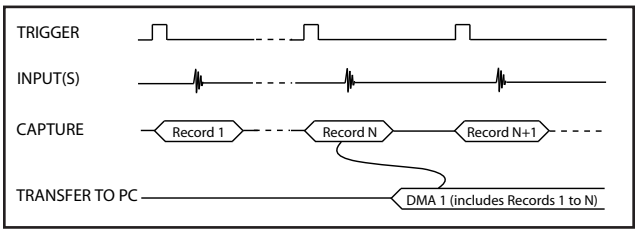
Recommended Motherboards or PCs

Many different types of motherboards and PCs have been benchmarked by AlazarTech. The ones that have produced the best throughput results are listed here: www.alazartech.com/images-media/2246-AlazarTechRecommendedMotherboards.pdf.

No Pre-Trigger (NPT) AutoDMA

Many ultrasonic scanning and medical imaging applications do not need any pre-trigger data: only post-trigger data is sufficient.

NPT AutoDMA is designed specifically for these applications. By only storing post-trigger data, the memory bandwidth is optimized and the entire on-board memory acts like a very deep FIFO.



Note that a DMA is not started until RecordsPerBuffer number of records (triggers) have been acquired and written to the on-board memory.

NPT AutoDMA buffers do not include headers. However, users can specify that each record should come with its own footer that contains a 40-bit trigger timestamp. The footer is called NPT Footer.

More importantly, a BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up. This provides a very substantial improvement over Traditional AutoDMA.

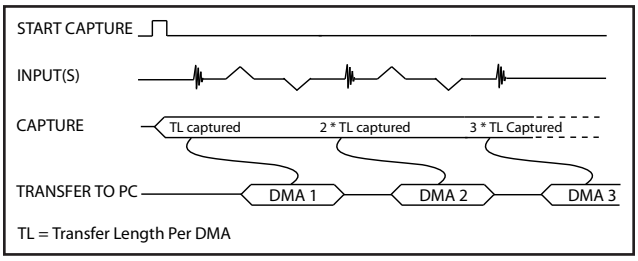
NPT AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow.

This is the recommended mode of operation for most ultrasonic scanning, OCT and medical imaging applications.

Continuous AutoDMA

Continuous AutoDMA is also known as the data streaming mode.

In this mode, data starts streaming across the PCIe bus as soon as the ATS9352 is armed for acquisition. It is important to note that triggering is disabled in this mode.



Continuous AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

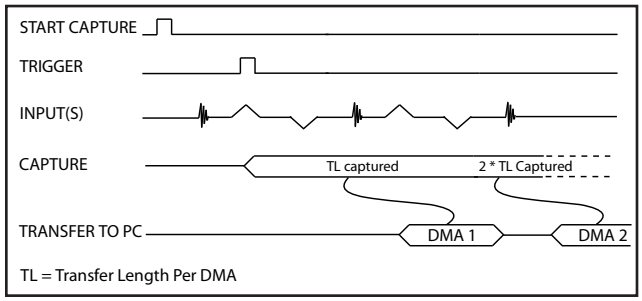
A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

The amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Continuous AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for very long signal recording.

Triggered Streaming AutoDMA

Triggered Streaming AutoDMA is virtually the same as Continuous mode, except the data transfer across the bus is held off until a trigger event has been detected.



Triggered Streaming AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

As in Continuous mode, the amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Triggered Streaming AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for RF signal recording that has to be started at a specific time, e.g. based on a GPS pulse.

Asynchronous DMA Driver

The various AutoDMA schemes discussed above provide hardware support for optimal data transfer. However, a corresponding high-performance software mechanism is also required to make sure sustained data transfer can be achieved.

This proprietary software mechanism is called Async DMA (short for Asynchronous DMA).

A number of data buffers are posted by the application software. Once a data buffer is filled, i.e. a DMA has been completed, ATS9352 hardware generates an interrupt, causing an event message to be sent to the ap-

plication so it can start consuming data. Once the data has been consumed, the application can post the data buffer back on the queue. This can go on indefinitely.

One of the great advantages of Async DMA is that almost 95% of CPU cycles are available for data processing, as all DMA arming is done on an event-driven basis.

To the best of our knowledge, no other supplier of waveform digitizers provides asynchronous software drivers. Their synchronous drivers force the CPU to manage data acquisition, thereby slowing down the overall data acquisition process.

Triggering

ATS9352 is equipped with sophisticated digital triggering options, such as programmable trigger thresholds and slope on any of the input channels or the External Trigger input.

While most oscilloscopes offer only one trigger engine, ATS9352 offers two trigger engines (called Engines J and K).

The user can specify the number of records to capture in an acquisition, the length of each record and the amount of pre-trigger data.

A programmable trigger delay can also be set by the user. This is very useful for capturing the signal of interest in a pulse-echo application, such as ultrasound, radar, lidar etc.

External Trigger Input

The external trigger input on the ATS9352 is labeled TRIG IN on the face plate.

By default, the input impedance of this input is 50 Ω and the full scale input range is +/- 3 Volts. The trigger signal is treated as an analog signal in this situation and a high-speed comparator receives the signal.

It is also possible to trigger the ATS9352 using a 3.3 V TTL signal. Input impedance is approximately 6.3 kΩ in this mode.

Timebase

ATS9352 timebase can be controlled either by on-board low-jitter VCO or by External Clock.

On-board low-jitter VCO uses an on-board 10 MHz TCXO as a reference clock.

External Clock

While the ATS9352 features low-jitter VCO and a 10 MHz TCXO as the source of the timebase system, there may be occasions when digitizing has to be synchronized to an external clock source.

ATS9352 External Clock feature provides an SMA input for an external clock signal, which should have a high slew rate. Signal levels, specified in detail on page 7, must be respected.

Input impedance for the External Clock input is fixed at 50 Ω. External clock input is always AC-coupled.

There are two types of External Clock supported by ATS9352. These are described below.

Fast External Clock

A new sample is taken by the on-board ADCs for each rising edge of this External Clock signal.

In order to satisfy the clocking requirements of the ADC chips being used, Fast External Clock frequency must always be higher than 25 MHz and lower than 500 MHz.

This is the ideal clocking scheme for OCT applications.

10 MHz Reference Clock

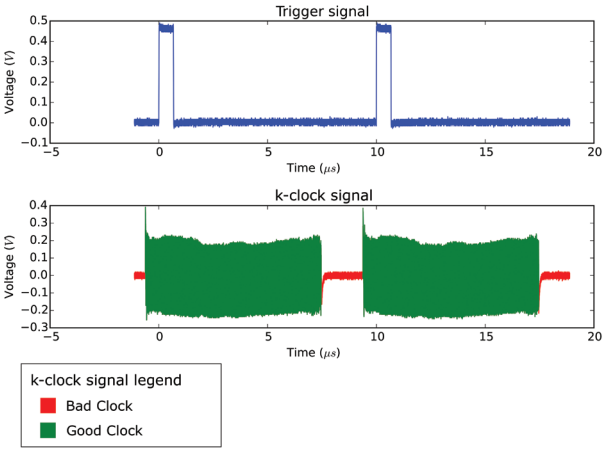
It is possible to generate the sampling clock based on an external 10 MHz reference input. This is useful for RF systems that use a common 10 MHz reference clock.

ATS9352 uses an on-board low-jitter VCO to generate the 500 MHz high-frequency clock used by the ADC. This 500 MHz sampling clock can then be decimated by a factor of 1, 2, 5, 10 or any other integer value that is divisible by 5.

OCT Ignore Bad Clock

The ADCs used on the ATS9352 require the external clock frequency to be above 150 MHz and lower than 500 MHz. In OCT applications, these limits cannot always be respected due to the nature of the optical source.

AlazarTech's *OCT Ignore Bad Clock* technology, allows safe operation with these out-of-specification clocks without requiring the use of a dummy clock in the source.



See www.alazartech.com/Technology/OCT-Ignore-Bad-Clock for more information on this technology.

AUX Connector

ATS9352 provides an AUX (Auxiliary) SMA connector that is configured as a Trigger Output connector by default.

When configured as a Trigger Output, AUX SMA connector outputs a 5 Volt TTL signal synchronous to the ATS9352 Trigger signal, allowing users to synchronize their test systems to the ATS9352 Trigger.

When combined with the Trigger Delay feature of the ATS9352, this option is ideal for ultrasonic and other pulse-echo imaging applications.

AUX connector can also be used as a Trigger Enable Input, or "Frame Start" input, which can be used to acquire complete frames, or B-scans, in imaging applications. In fact, this is the most popular use of the AUX connector in OCT applications.

Calibration

Every ATS9352 digitizer is factory calibrated to NIST- and CNRC-traceable standards. To recalibrate an ATS9352, the digitizer must be shipped back to the factory.

On-Board Monitoring

Adding to the reliability offered by ATS9352 are the on-board diagnostic circuits that constantly monitor over 20 different voltages, currents and temperatures. LED alarms are activated if any of the values surpass the limits.

AlazarDSO Software

ATS9352 is supplied with the powerful AlazarDSO software that allows the user to setup the acquisition hardware and capture, display and archive the signals.

The Stream-To-Memory command in AlazarDSO allows users to stream a large dataset to motherboard memory.

AlazarDSO software also includes powerful tools for benchmarking the computer bus and disk drive.

Software Development Kits

AlazarTech provides an easy-to-use software development kit for customers who want to integrate the ATS9352 into their own software.

A Windows and Linux compatible software development kit, called ATS-SDK, includes headers, libraries and source code sample programs written in C/C++, C#, Python, MATLAB, and LabVIEW. These programs can fully control the ATS9352 and acquire data in user buffers.

The purchase of an ATS-SDK license includes a subscription that provides the following benefits for a period of 12 months from the date of purchase:

- Download ATS-SDK updates from the AlazarTech website;
- Receive technical support on ATS-SDK.

Customers who want to receive technical support and download new releases beyond this 12 month period should purchase extended support and maintenance (order number ATS-SDK-1YR).

ATS-GPU

ATS-GPU is a software library developed by AlazarTech to allow users to do real-time data transfer from ATS9352 to a GPU card at rates up to 1.6 GB/s.

Modern GPUs include very powerful processing units and a very high-speed graphical memory bus. This combination makes them perfectly suited for signal processing applications.

ATS-GPU-BASE is supplied with an example user application in source code. The application includes GPU kernels that use ATS-GPU to receive data, do very simple signal processing (data inversion), and copy the processed (inverted) data back to a user buffer. All this is done at the highest possible data transfer rate.

Programmers can replace the data inversion code with application-specific signal processing kernels to develop custom applications.

ATS-GPU-OCT is the optional OCT Signal Processing library for ATS-GPU. It contains floating-point FFT routines that have also been optimized to provide the maximum number of FFTs per second. Kernel code running on the GPU can do zero-padding, apply a windowing function, do a floating-point FFT, calculate the amplitude and convert the result to a log scale. It is also possible to output phase information.

FFTs can be done on triggered data or on continuous gapless stream of data. It is also possible to do spectral averaging.

ATS-GPU supports 64-bit Windows and 64-bit Linux for CUDA®-based development.

Support for Windows

Windows support for ATS9352 includes Windows 10, Windows 8.x, Windows 7 SP1 with security update KB3033929 (SHA-2 Code Signing Support), Windows Server 2012, Windows Server 2010, and Windows Server 2008 R2.

Microsoft support for Windows 7 and Windows Server 2008 R2 ended on January 14, 2020. As such, AlazarTech is ceased development on Windows 7 and Windows Server 2008 R2 as of this date. We will continue to support customers using Windows 7 and Windows Server 2008 R2 until December 31, 2020. After this date, no support will be provided.

Due due to lack of demand and due to the fact that Microsoft no longer supports these operating systems, AlazarTech no longer supports Windows XP, Windows Vista, and Windows Server 2008.

Linux Support

AlazarTech offers ATS9352 binary drivers for the following Linux distributions: CentOS, Debian, and Ubuntu.

Users can download the binary driver for their specific distribution by choosing from the available drivers here:

ftp://release@ftp.alazartech.com/outgoing/linux

Also provided is a GUI application called AlazarFrontPanel that allows simple data acquisition and display.

ATS-SDK includes source code example programs for Linux, which demonstrate how to acquire data programmatically using a C compiler.

If customers want to use ATS9352 in any Linux distribution other than the ones listed above, they can have the AlazarTech engineering team generate an appropriate driver for a nominal fee, if applicable.

Based on a minimum annual business commitment, the Linux driver source code license (order number ATS9352-LINUX) may be granted to qualified OEM customers for a fee. For release of driver source code, a Non-Disclosure Agreement must be executed between the customer's organization and AlazarTech.

All such source code disclosures are made on an as-is basis with limited support from the factory.

Extended Warranty

The purchase of an ATS9352 includes a standard one (1) year parts and labor warranty. Customers may extend their warranty by ordering the Extended Warranty (order number ATS9352-061).

This must be purchased before expiration of the standard warranty (or before expiration of an Extended Warranty). Extended Warranties can only be purchased while there is a valid warranty in place.

AlazarTech reserves the right to limit the number of warranty extensions for any product.

Get your warranty end date by registering your product at: www.alazartech.com/UserHome?tab=2.

OEM Packaging

ATS9352 is available in OEM quantities. All OEM-quantity orders are delivered in a single shipment (no partial shipments allowed). OEM-quantity orders (order numbers ATS9352-110, ATS9352-125, ATS9352-150, ATS9352-200) come in OEM packaging, which does not include software and documentation on USB flash drive.

Software and documentation must be downloaded from www.alazartech.com/Support/Downloads.

Export Control Classification

According to the *Export Controls Division of the Government of Canada*, ATS9352 is currently not controlled for export from Canada. Its export control classification is N8, which is equivalent to ECCN EAR99.

ATS9352 can be shipped freely outside of Canada, with the exception of countries listed on the *Area Control List* and *Sanctions List*. Furthermore, if the end-use of ATS9352, in part or in its entirety, is related to the development or deployment of weapons of mass destruction, AlazarTech is obliged to apply for an export permit.

RoHS Compliance

ATS9352 is fully RoHS compliant, as defined by Directive 2015/863/EU (RoHS 3) of the European Parliament and of the Council of 31 March 2015 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

All manufacturing is done using RoHS-compliant components and lead-free soldering.

EC Conformity

ATS9352 conforms to the following standards:

Electromagnetic Emissions:
CISPR 22:2006/EN 55022:2006 (Class A):
Information Technology Equipment (ITE). Radio disturbance characteristics. Limits and method of measurement.

Electromagnetic Immunity:
CISPR 24:1997/EN 55024:1998 (+A1 +A2):
Information Technology Equipment Immunity characteristics — Limits and methods of measurement.

Safety:
IEC 60950-1:2005: Information technology equipment — Safety — Part 1: General requirements.

IEC 60950-1:2006: Information technology equipment — Safety — Part 1: General requirements.

ATS9352 also follows the provisions of the following directives: 2006/95/EC (Low Voltage Equipment); 2004/108/EC (Electromagnetic Compatibility).

FCC & ICES-003 Compliance

ATS9352 has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15, subpart B of the FCC Rules, and the Canadian Interference-Causing Equipment Standard ICES-003:2004.

† AlazarDSO, AlazarTech, and AlazarTech ATS are registered trademarks of Alazar Technologies Inc.
MATLAB is a trademark and/or registered trademark of The MathWorks, Inc.
LabVIEW is a trademark and/or registered trademark of National Instruments.
Windows and Windows Server are trademarks and/or registered trademarks of Microsoft Corporation in the U.S. and/or other countries.
Linux is a registered trademark of Linus Torvalds.
CUDA is a trademarks and/or registered trademark of NVIDIA Corporation in the U.S. and/or other countries.
All other trademarks are the property of their respective owners.

ATS9352

500 MS/s 12-Bit PCI Express Digitizer

System Requirements

Personal computer with at least one free x4, x8, or x16 PCI Express (v2.0) slot, 2 GB RAM, 100 MB of free hard disk space, SVGA display adaptor and monitor with at least a 1024 x 768 resolution.

Power Requirements

+12 V	1.2 A, typical
+3.3 V	1.1 A, typical

Physical

Size	Single slot, half length PCI Express card (4.377 inches x 6.5 inches excluding the connectors protruding from the front panel)
Weight	250 g

I/O Connectors

ECLK, CH A, CH B, TRIG IN, AN IN, AUX I/O	SMA female connectors

Environmental

Operating temperature	0 to 55 degrees Celsius
Storage temperature	-20 to 70 degrees Celsius
Relative humidity	5 to 95%, non-condensing

Acquisition System

Resolution	12 bits
Bandwidth (-3 dB)	
DC-coupled, 50 Ω	DC - 250 MHz
AC-coupled, 50 Ω	100 kHz - 250 MHz
Number of channels	2, simultaneously sampled
Maximum sample rate	500 MS/s single shot
Minimum sample rate	1 KS/s single shot for internal clocking
Full scale input ranges	
50 Ω input impedance:	±100 mV, ±200 mV, ±400 mV, ±1 V, ±2 V, and ±4 V, software-selectable
DC accuracy	±2% of full scale in all ranges
Input coupling	AC or DC, software-selectable
Input impedance	50 Ω ±1%
Input protection	
50 Ω	±4 V (DC + peak AC for CH A, CH B, and TRIG IN only without external attenuation)

Additional Low-Frequency Analog Input

Bandwidth (-3 dB)	
DC-coupled, 50 Ω	DC - 100 kHz
Maximum sample rate	200 KS/s single shot
Full scale input range	-0.5 V to +2.5 V, fixed
DC accuracy	±2% of full scale in all ranges
Input coupling	DC
Input impedance	50 Ω ±1%
Input protection	±3 V
Absolute max. amplitude	5 V_{P-P}

Acquisition Memory System

Acquisition Memory/ch	128 Million samples per channel
Record length	Software-selectable with 32-point resolution. Record length must be a minimum of 256 points. There is no upper limit on the maximum record length.
Number of records	Software-selectable from a minimum of 1 to a maximum of infinite number of records
Pre-trigger depth	From 0 to 4080 for single channel From 0 to 2040 for dual channel
Post-trigger depth	Record Length – Pre-Trigger Depth

Timebase System

Timebase options	Internal Clock or External Clock
Internal sample rates	500 MS/s, 250 MS/s, 100 MS/s, 50 MS/s, 20 MS/s, 10 MS/s, 5 MS/s, 2 MS/s, 1 MS/s, 500 KS/s, 200 KS/s, 100 KS/s, 50 KS/s, 20 KS/s, 10 KS/s, 5 KS/s, 2 KS/s, 1 KS/s
Internal clock accuracy	±2 ppm

Dynamic Parameters

Typical values measured on the 400 mV range of CH A of a randomly selected ATS9352. Input signal was provided by a Rohde & Schwarz SMB100A signal generator, followed by a 9-pole, 10 MHz band-pass filter (TTE Q36T-10M-1M-50-720BMF). Input frequency was set at 9.9 MHz and output amplitude was 270 mV rms, which was approximately 95% of the full scale input.

SNR	53.43 dB
SINAD	53.90 dB
THD	-64.33 dB
SFDR	68.5 dBc

Note that these dynamic parameters may vary from one unit to another, with input frequency and with the full scale input range selected.

ECLK (External Clock) Input

Signal level	250 mV_{P-P} to 2 V_{P-P}
Input impedance	50 Ω
Input coupling	AC
Maximum frequency	500 MHz for Fast External Clock
Minimum frequency	25 MHz for Fast External Clock
Sampling edge	Rising

10 MHz Reference PLL Input

Signal level	200 mV_{P-P} to 2 V_{P-P}
Input impedance	50 Ω
Input coupling	AC
Input frequency	10 MHz ± 0.1 MHz
Maximum frequency	10.1 MHz
Minimum frequency	9.9 MHz
Sampling clock freq.	500 MHz

ATS9352
500 MS/s 12-Bit PCI Express Digitizer

Triggering System

Mode	Edge triggering with hysteresis
Comparator type	Digital comparators for internal (CH A, CH B) triggering and software-selectable analog comparators or TTL gate for TRIG IN (External) triggering
Number of trigger engines	2
Trigger engine combination	Engine J, engine K, J OR K, software-selectable
Trigger engine source	CH A, CH B, TRIG IN, Software or None, independently software-selectable for each of the two Trigger Engines
Hysteresis	±5% of full scale input, typical
Trigger sensitivity	±10% of full scale input range, except for TTL triggering for External Trigger. This implies that the trigger system may not trigger reliably if the input has an amplitude less than ±10% of full scale input range selected
Trigger level accuracy	±5%, typical, of full scale input range of the selected trigger source
Bandwidth	250 MHz
Trigger delay	Software-selectable from 0 to 9,999,999 sampling clock cycles
Trigger timeout	Software-selectable with a 10 µs resolution. Maximum settable value is 3,600 seconds. Can also be disabled to wait indefinitely for a trigger event

TRIG IN (External Trigger) Input

Input type	Analog or 3.3 V TTL (5 V compliant), software-selectable
Input coupling	DC only
Analog input impedance	50 Ω
Analog bandwidth (-3 dB)	DC - 250 MHz
Analog input range	±3 V
Analog DC accuracy	±10% of full scale input
Analog input protection	±8 V (DC + peak AC without external attenuation)
TTL input impedance	6.3 kΩ ±10%
TTL min. pulse width	32 ADC sampling clocks
TTL min. pulse amplitude	2 Volts
TTL input protection	-0.7 V to + 5.5 V

Auxiliary I/O (AUX I/O)

Signal direction	Input or Output, software-selectable. Trigger Output by default
Output types:	Trigger Output, Pacer (programmable clock) Output, Software-controlled Digital Output
Input types:	Trigger Enable Software readable Digital Input
Output	
Amplitude:	5 Volt TTL
Synchronization:	Synchronized to a clock derived from the ADC sampling clock. Divide-by-4 clock (dual channel mode) or divide-by-8 clock (single channel mode)
Input	
Amplitude:	3.3 Volt TTL (5 Volt compliant)

Materials Supplied

ATS9352 PCI Express card

ATS9352 Installation Disk (on USB Flash Drive)‡

Certification and Compliances

RoHS 3 (Directive 2015/863/EU) Compliance

CE Marking — EC Conformity

FCC Part 15 Class A / ICES-003 Class A Compliance

All specifications are subject to change without notice

‡ *Only applies to order number ATS9352-001. USB flash drive is not provided for OEM-quantity orders (order numbers ATS9352-110, ATS9352-125, ATS9352-150, and ATS9352-200). For OEM-quantity orders, software must be downloaded from www.alazartech.com/Support/Downloads.*

ORDERING INFORMATION

ATS9352 (single unit)	ATS9352-001
ATS9352: One Year Extended Warranty	ATS9352-061
ATS9352 (10-24 units)	ATS9352-110
ATS9352 (25-49 units)	ATS9352-125
ATS9352 (50-99 units)	ATS9352-150
ATS9352 (100+ units)	ATS9352-200
Software Development Kit 1 Year Subscription (Supports C/C++, Python, MATLAB, and LabVIEW)	ATS-SDK
ATS-GPU-BASE: GPU Streaming Library 1 Year Subscription	ATSGPU-001
ATS-GPU-OCT: Signal Processing Library 1 Year Subscription (requires ATSGPU-001)	ATSGPU-101

Manufactured By:

Alazar Technologies, Inc.

6600 TRANS-CANADA HIGHWAY, SUITE 310
POINTE-CLAIRE, QC, CANADA H9R 4S2

TOLL FREE: 1-877-7-ALAZAR OR 1-877-725-2927
TEL: (514) 426-4899 FAX: (514) 426-2723

E-MAIL: sales@alazartech.com

DATASHEET REVISION HISTORY

Changes from version 1.1 (Nov 2019) to version 1.1a	Section, Page
Added *Gen 2* to *Bus* column	Feature Table, pg. 1
Added AlazarFrontPanel (for Linux) as benchmarking tool	Maximum Sustained Transfer Rate, pg. 2
Because signal levels differ for Fast External Clock and 10 MHz Reference Clock, replaced min. and max. amplitude with a note that signal levels specified on page 7 must be respected.	External Clock, pg. 4
Added end-of-support notice for Windows 7 and Windows Server 2008 R2	Support for Windows, pg. 5
Changed signal level from "500 mV_{P-P} to 2 V_{P-P}" to "250 mV_{P-P} to 2 V_{P-P}"	ECLK (External Clock) Input, pg. 7
Changed signal level from "500 mV_{P-P} to 2 V_{P-P}" to "200 mV_{P-P} to 2 V_{P-P}"	10 MHz Reference PLL Input, pg. 7
Updated product names for: ATS9352-001, ATS9352-110, ATS9352-125, ATS9352-150, ATS9352-200	Ordering Information, pg. 8