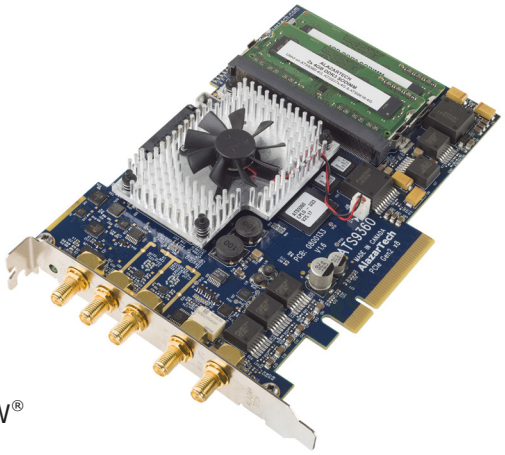
ATS9360

1.8 GS/s 12-Bit PCIe Gen2 Digitizer

- 3.5 GB/s PCIe Gen 2 (8-lane) interface
- 2 channels sampled at 12-bit resolution
- 1.8 GS/s real-time sampling rate
- FPGA-based FFT processing
- Variable frequency external clocking
- Continuous streaming mode
- ±400 mV fixed input range
- Asynchronous DMA device driver
- AlazarDSO® oscilloscope software
- Software Development Kit supports C/C++, C#, Python, MATLAB®, LabVIEW®
- Support for Windows® & Linux®



RoHS 3 COMPLIANT
2015/863/EU

CE

Product	Bus	Operating System	Channels	Max. Sample Rate	Bandwidth	Memory Per Channel	Resolution
ATS9360	PCIe x8 Gen 2	32-bit/64-bit Windows & 64-bit Linux	2	1.8 GS/s	800 MHz	2/4 Gigasamples in dual/single channel mode	12 bits

Overview

AlazarTech ATS®9360 is an 8-lane PCI Express Gen 2 (PCIe x8), dual-channel, high-speed, 12-bit, 1.8 GS/s waveform digitizer card capable of streaming acquired data to PC memory at rates up to 3.5 GB/s.

It is also possible to do FPGA-based 4096-point FFT on acquired data. This is useful for Optical Coherence Tomography (OCT) related applications.

Unlike other products on the market, ATS9360 does not use interleaved sampling. Each input has its own 12-bit, 1.8 GSPS ADC chip.

Optional variable frequency external clock allows operation from 1.8 GHz down to 300 MHz (or 75 MHz for screened ATS9360 cards), making ATS9360 an ideal waveform digitizer for OCT applications.

Users can capture data from one trigger or a burst of triggers. Users can also stream very large datasets continuously to PC memory or hard disk.

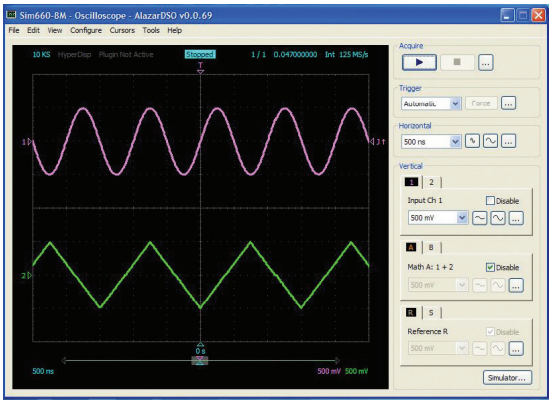
ATS9360 is supplied with AlazarDSO software that lets the user get started immediately without having to go through a software development process.

Users who need to integrate the ATS9360 in their own program can purchase a software development kit, ATS-SDK, for C/C++, C#, Python, MATLAB, and LabVIEW for both Windows and Linux operating systems.

All of this advanced functionality is packaged in a low power, half-length PCI Express card.

Applications

Optical Coherence Tomography (OCT)
Ultrasonic & Eddy Current NDT/NDE
RF Signal Recording & Analysis
Terabyte Storage Oscilloscope
High-Resolution Oscilloscope
Spectroscopy
Multi-Channel Transient Recording



ATS9360
1.8 GS/s 12-Bit PCIe Gen2 Digitizer

PCI Express Bus Interface
ATS9360 interfaces to the host computer using an 8-lane PCI Express bus. Each lane operates at 5.0 Gbps (Gen 2).

According to PCIe specification, an 8-lane board can be plugged into any 8-lane or 16-lane slot, but not into a 4-lane or 1-lane slot. As such, ATS9360 requires at least one free 8-lane or 16-lane slot on the motherboard.

The physical and logical PCIe x8 interface is provided by an on-board FPGA, which also integrates acquisition control functions, memory management functions and acquisition datapath. This very high degree of integration maximizes product reliability.

The AlazarTech® 3.5 GB/s benchmark was done on ASUS P9X79 Pro and X99 Deluxe motherboards.

Users must always be wary of throughput specifications from manufacturers of waveform digitizers. Some unscrupulous manufacturers tend to specify the raw, burst-mode throughput of the bus. AlazarTech, on the other hand, specifies the benchmarked sustained throughput. To achieve such high throughput, a great deal of proprietary memory management logic and kernel mode drivers have been designed.

Analog Input
An ATS9360 features two analog input channels. Each channel has up to 800 MHz of full power analog input bandwidth. Input voltage range is fixed at ±400 mV.

It must be noted that input impedance of both channels is fixed at 50 Ω. Input coupling is fixed to DC.

Acquisition System
ATS9360 PCI Express digitizers use state-of-the-art 1.8 GS/s, 12-bit ADCs to digitize the input signals. The real-time sampling rate ranges from 1.8 GS/s down to 1 KS/s for internal clock and 300 MS/s for external clock.

The two channels are guaranteed to be simultaneous, as the two ADCs use a common clock.

An acquisition can consist of multiple records, with each record being captured as a result of one trigger event. A record can contain both pre-trigger and post-trigger data.

Infinite number of triggers can be captured by ATS9360.

In between the multiple triggers being captured, the acquisition system is re-armed by the hardware within 256 sampling clock cycles.

This mode of capture, sometimes referred to as Multiple Record, is very useful for capturing data in applications with a very rapid or unpredictable trigger rate. Examples of such applications include medical imaging, ultrasonic testing, OCT and NMR spectroscopy.

On-Board Acquisition Memory
ATS9360 has 8 GB of on-board memory, which is used as a very deep FIFO between the A/D converters and PCI Express bus. This memory is necessary to accommodate any temporary pauses in data transfer caused by the motherboard or the operating system.

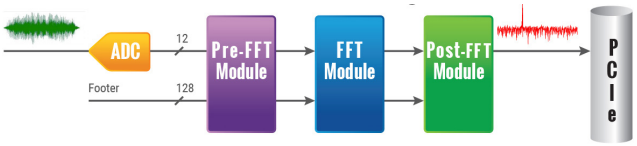
Maximum Sustained Transfer Rate
PCI Express support on different motherboards is not always the same, resulting in significantly different sustained data transfer rates. The reasons behind these differences are complex and varied and will not be discussed here.

ATS9360 users can quickly determine the maximum sustained transfer rate for their motherboard by inserting their card in a PCIe slot and running the bus benchmarking tool provided in AlazarDSO for Windows or AlazarFrontPanel for Linux.

Recommended Motherboards or PCs
Many different types of motherboards and PCs have been benchmarked by AlazarTech. The ones that have produced the best throughput results (3.5 GB/s) are listed here: www.alazartech.com/images-media/2246-AlazarTechRecommendedMotherboards.pdf.

AlazarTech recommends that customers not use SandyBridge CPUs with ATS9360.

FPGA-Based FFT Processing
It is now possible to do real-time FFT signal processing using the on-board FPGA. Note that only one input can be processed.



Up to 4096-point FFT length is supported. A user programmable complex windowing function can be applied to the acquired data before FFT calculation.

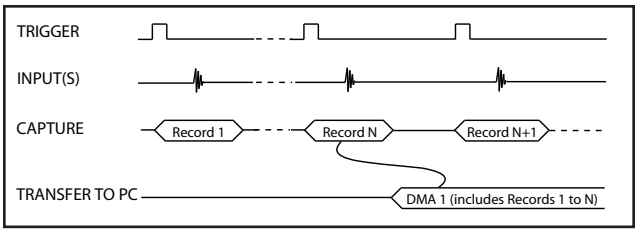
The complex FFT output is converted to magnitude in single-precision floating-point format. A logarithmic output is also available.

It is also possible to DMA both frequency and time domain data. This allows users to verify FPGA-based FFT operation during algorithm development.

ATS9360 can perform 200,000 4096-point FFTs per second.

FPGA-based FFT is ideal for customers in the Optical Coherence Tomography (OCT) field.

No Pre-Trigger (NPT) AutoDMA
Many ultrasonic scanning and medical imaging applications do not need any pre-trigger data: only post-trigger data is sufficient.



NPT AutoDMA is designed specifically for these applications. By only storing post-trigger data, the memory bandwidth is optimized and the entire on-board memory acts like a very deep FIFO.

Note that a DMA is not started until RecordsPerBuffer number of records (triggers) have been acquired and written to the on-board memory.

Starting with FPGA version 19.02, NPT AutoDMA buffers can include a footer that contains trigger time-stamp and other information about that particular record. The footer is called NPT Footer.

A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

NPT AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow.

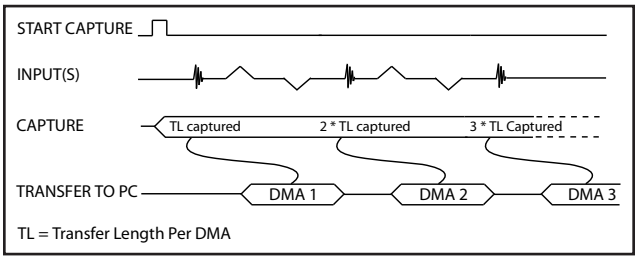
This is the recommended mode of operation for most ultrasonic scanning, OCT and medical imaging applications.

It should be noted that even though this mode is called "No Pre Trigger", it is now possible to do limited pre-trigger data captures of up to 8192 points in single channel mode and 4096 points in dual channel mode.

Continuous AutoDMA

Continuous AutoDMA is also known as the data streaming mode.

In this mode, data starts streaming across the PCIe bus as soon as the ATS9360 is armed for acquisition. It is important to note that triggering is disabled in this mode.



Continuous AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

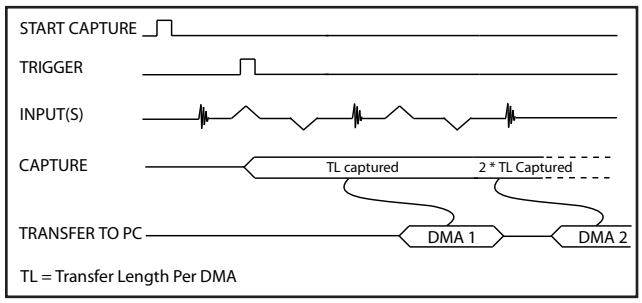
A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

The amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Continuous AutoDMA can easily acquire data to PC host memory at the maximum possible rate allowed by the motherboard. This is the recommended mode for very long signal recording.

Triggered Streaming AutoDMA

Triggered Streaming AutoDMA is virtually the same as Continuous mode, except the data transfer across the bus is held off until a trigger event has been detected.



Triggered Streaming AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

As in Continuous mode, the amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Triggered Streaming AutoDMA can easily acquire data to PC host memory at the maximum possible rate allowed by the motherboard. This is the recommended mode for RF signal recording that has to be started at a specific time, e.g. based on a GPS pulse.

Data Packing Mode

By default, ATS9360 stores 12-bit data acquired by its on-board A/D converters as a 16-bit integer. Users can also choose to pack the data as 12-bit integers or even 8-bit integers. Being able to reduce the total amount of data being transferred can be very useful in data recording applications.

Note that it is the user application's responsibility to unpack the data. Also note that NPT Footers are not available in Data Packing Mode.

Asynchronous DMA Driver

The various AutoDMA schemes discussed above provide hardware support for optimal data transfer. However, a corresponding high-performance software mechanism is also required to make sure sustained data transfer can be achieved.

This proprietary software mechanism is called Async DMA (short for Asynchronous DMA).

A number of data buffers are posted by the application software. Once a data buffer is filled, i.e. a DMA has been completed, ATS9360 hardware generates an interrupt,

causing an event message to be sent to the application so it can start consuming data. Once the data has been consumed, the application can post the data buffer back on the queue. This can go on indefinitely.

One of the great advantages of Async DMA is that almost 95% of CPU cycles are available for data processing, as all DMA arming is done on an event-driven basis.

To the best of our knowledge, no other supplier of waveform digitizers provides asynchronous software drivers. Their synchronous drivers force the CPU to manage data acquisition, thereby slowing down the overall data acquisition process.

Triggering

ATS9360 is equipped with sophisticated digital triggering options, such as programmable trigger thresholds and slope on any of the input channels or the External Trigger input.

While most oscilloscopes offer only one trigger engine, ATS9360 offers two trigger engines (called Engines J and K).

The user can specify the number of records to capture in an acquisition, the length of each record and the amount of pre-trigger data.

A programmable trigger delay can also be set by the user. This is very useful for capturing the signal of interest in a pulse-echo application, such as ultrasound, radar, lidar etc.

External Trigger Input

ATS9360 external trigger input (TRIG IN) can be set as an analog input with ±2.5 V full scale input range and 50 Ω input impedance, or a 3.3 V TTL (5 V-compliant) input.

When TTL input is selected, the input impedance increases to approximately 6.7 kΩ, making it easier to drive the TRIG IN input from high-output impedance sources.

Note: If full 12-bit resolution is required, users should select CH A or CH B as the trigger source. When the External Trigger Input is used as the trigger source, the least significant bit (LSB) of each 12-bit sample is replaced by the state of the external trigger signal source.

Timebase

ATS9360 timebase can be controlled either by on-board low-jitter VCO or by optional External Clock.

On-board low-jitter VCO uses an on-board 10 MHz TCXO as a reference clock. Clock buffers used feature less than 76 fs_{RMS} additive jitter.

Optional External Clock

While the ATS9360 features low jitter VCO and a 10 MHz TCXO as the source of the timebase system, there may be occasions when digitizing has to be synchronized to an external clock source.

ATS9360 External Clock option provides an SMA input for an external clock signal, which should have a high slew rate. Signal levels, specified in detail on page 7, must be respected.

Input impedance for the External Clock input is fixed at 50 Ω. External clock input is always AC-coupled.

There are two types of External Clock supported by ATS9360. These are described below.

Fast External Clock

A new sample is taken by the on-board ADCs for each rising edge of this External Clock signal.

In order to satisfy the clocking requirements of the ADC chips being used, Fast External Clock frequency must always be higher than 300 MHz and lower than 1.8 GHz.

For customers whose external clocks may go lower than 300 MHz during the acquisition, it is possible to have AlazarTech screen the ATS9360 boards for external clock operation down to 75 MHz (Order number ATS9360-006).

This is the ideal clocking scheme for OCT applications.

10 MHz Reference Clock

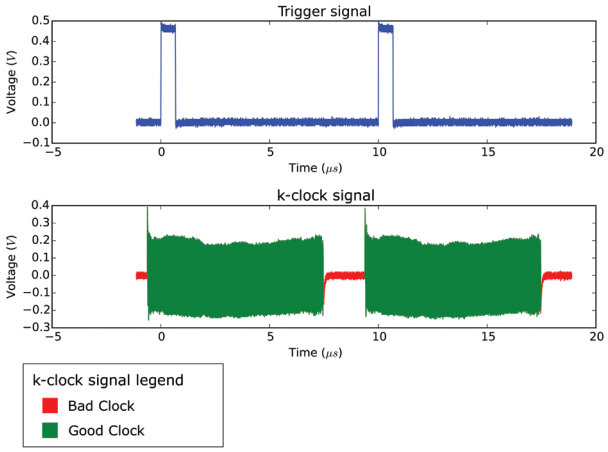
It is possible to generate the sampling clock based on an external 10 MHz reference input. This is useful for RF systems that use a common 10 MHz reference clock.

ATS9360 uses an on-board low-jitter VCO to generate a user-specified high-frequency clock used by the ADC. This sampling clock can be virtually any multiple of 1 MHz.

OCT Ignore Bad Clock

The ADCs used on the ATS9360 require the external clock frequency to be above 300 MHz and lower than 1.8 GHz. In OCT applications, these limits cannot always be respected due to the nature of the optical source.

AlazarTech's *OCT Ignore Bad Clock* technology allows safe operation with these out-of-specification clocks without requiring the use of a dummy clock in the source.



Firmware version 19.09+, driver version 5.10.6+ and SDK 7.1.3+ are required to take advantage of OCT Ignore Bad Clock. For existing customers, these firmware and driver versions are available for download from AlazarTech's website free of charge.

See www.alazartech.com/Technology/OCT-Ignore-Bad-Clock for more information on this technology.

AUX Connector

ATS9360 provides an AUX (Auxiliary) SMA connector that is configured as a Trigger Output connector by default.

When configured as a Trigger Output, AUX SMA connector outputs a 5 Volt TTL signal synchronous to the ATS9360 Trigger signal, allowing users to synchronize their test systems to the ATS9360 Trigger.

When combined with the Trigger Delay feature of the ATS9360, this option is ideal for ultrasonic and other pulse-echo imaging applications.

AUX connector can also be used as a Trigger Enable input for frame (B-scan) capture applications. In fact, this is the most popular use of the AUX connector in OCT applications.

Calibration

Every ATS9360 digitizer is factory calibrated to NIST- or CNRC-traceable standards. To recalibrate an ATS9360, the digitizer must be shipped back to the factory.

On-Board Monitoring

Adding to the reliability offered by ATS9360 are the on-board diagnostic circuits that constantly monitor over 20 different voltages, currents and temperatures. LED alarms are activated if any of the values surpass the limits.

AlazarDSO Software

ATS9360 is supplied with the powerful AlazarDSO software that allows the user to setup the acquisition hardware and capture, display and archive the signals.

The Stream-To-Memory command in AlazarDSO allows users to stream a large dataset to motherboard memory.

AlazarDSO software also includes powerful tools for benchmarking the computer bus and disk drive.

Software Development Kits

AlazarTech provides an easy to use software development kit for customers who want to integrate the ATS9360 into their own software.

A Windows and Linux compatible software development kit, called ATS-SDK, includes headers, libraries and source code sample programs written in C/C++, C#, Python, MATLAB, and LabVIEW. These programs can fully control the ATS9360 and acquire data in user buffers.

The purchase of an ATS-SDK license includes a subscription that provides the following benefits for a period of 12 months from the date of purchase:

- Download ATS-SDK updates from the AlazarTech website;
- Receive technical support on ATS-SDK.

Customers who want to receive technical support and download new releases beyond this 12 month period should purchase extended support and maintenance (order number ATS-SDK-1YR).

ATS-GPU

ATS-GPU is a software library developed by AlazarTech to allow users to do real-time data transfer from ATS9360 to a GPU card at rates up to 3.5 GB/s.

Modern GPUs include very powerful processing units and a very high-speed graphical memory bus. This combination makes them perfectly suited for signal processing applications.

ATS-GPU-BASE is supplied with an example user application in source code. The application includes GPU kernels that use ATS-GPU to receive data, do very simple signal processing (data inversion), and copy the processed (inverted) data back to a user buffer. All this is done at the highest possible data transfer rate.

Programmers can replace the data inversion code with application-specific signal processing kernels to develop custom applications.

ATS-GPU-OCT is the optional OCT Signal Processing library for ATS-GPU. It contains floating-point FFT routines that have also been optimized to provide the maximum number of FFTs per second. Kernel code running on the GPU can do zero-padding, apply a windowing function, do a floating-point FFT, calculate the amplitude and convert the result to a log scale. It is also possible to output phase information.

FFTs can be done on triggered data or on continuous gapless stream of data. It is also possible to do spectral averaging. Our benchmarks showed that it was possible to do 1,130,000 FFTs per second when capturing data in dual-channel mode and using a NVIDIA® Quadro® P5000 GPU.

ATS-GPU supports 64-bit Windows 64-bit and Linux for CUDA®-based development.

Support for Windows

Windows support for ATS9360 includes Windows 10, Windows 8.x, Windows 7 SP1 with update KB3033929 (SHA-2 Code Signing Support), Windows Server 2012, Windows Server 2010, and Windows Server 2008 R2.

Microsoft support for Windows 7 and Windows Server 2008 R2 ends on January 14, 2020. As such, AlazarTech is ceasing development on Windows 7 and Windows Server 2008 R2 as of this date. We will continue to sup-

port customers using Windows 7 and Windows Server 2008 R2 until December 31, 2020. After this date, no support will be provided.

Due due to lack of demand and due to the fact that Microsoft no longer supports these operating systems, AlazarTech no longer supports Windows XP, Windows Vista, and Windows Server 2008.

Support for Linux

AlazarTech offers ATS9360 binary drivers for the following Linux distributions: CentOS, Debian, and Ubuntu.

Users can download the binary driver for their specific distribution by choosing from the available drivers here:

ftp://release@ftp.alazartech.com/outgoing/linux

Also provided is a GUI application called AlazarFrontPanel that allows simple data acquisition and display.

ATS-SDK includes source code example programs for Linux, which demonstrate how to acquire data programmatically using a C compiler.

If customers want to use ATS9360 in any Linux distribution other than the ones listed above, they can have the AlazarTech engineering team generate an appropriate driver for a nominal fee, if applicable.

Based on a minimum annual business commitment, the Linux driver source code license (order number ATS9360-LINUX) may be granted to qualified OEM customers for a fee. For release of driver source code, a Non-Disclosure Agreement must be executed between the customer's organization and AlazarTech.

All such source code disclosures are made on an as-is basis with limited support from the factory.

Extended Warranty

The purchase of an ATS9360 includes a standard one (1) year parts and labor warranty. Customers may extend their warranty by ordering an Extended Warranty (order number ATS9360-061).

This must be purchased before expiration of the standard warranty (or before expiration of an Extended Warranty). Extended Warranties can only be purchased while there is a valid warranty in place. AlazarTech reserves the right to limit the number of warranty extensions for any product.

Get your warranty end date by registering your product at: www.alazartech.com/UserHome?tab=2.

Export Control Classification

According to the latest *Export and brokering controls handbook*, amended August 2019, ATS9360 is classified by the Export Controls Division of the Government of Canada as a controlled product under ECL 1-3.A.2.h, which is equivalent to ECCN 3A002.h.

For sales where the ultimate country destination is Canada or U.S., no export permit is required unless the end-use of ATS9360, in part or in its entirety, is related to the development or deployment of weapons of mass destruction.

For shipments to eligible destinations, AlazarTech is allowed to export under a general export permit, unless the end-use of ATS9360, in part or in its entirety, is related to the development or deployment of weapons of mass destruction. For general export permit shipments, users must provide a signed export compliance statement (ECS) that includes a detailed description of the end-use. Shipments cannot be made without a signed ECS on file.

For all other countries, and for all cases where the end-use of ATS9360, in part or in its entirety, is related to the development or deployment of weapons of mass destruction, an export permit is required, which will require extensive details on the end-use and end-users. This process may cause significant delays.

RoHS Compliance

ATS9360 is fully RoHS compliant, as defined by Directive 2015/863/EU (RoHS 3) of the European Parliament and of the Council of 31 March 2015 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

All manufacturing is done using RoHS-compliant components and lead-free soldering.

EC Conformity

ATS9360 conforms to the following standards:

Electromagnetic Emissions:
CISPR 22:2006/EN 55022:2006 (Class A):
Information Technology Equipment (ITE). Radio disturbance characteristics. Limits and method of measurement.

Electromagnetic Immunity:
CISPR 24:1997/EN 55024:1998 (+A1 +A2):
Information Technology Equipment Immunity characteristics — Limits and methods of measurement.

Safety:
IEC 60950-1:2005: Information technology equipment — Safety — Part 1: General requirements.

IEC 60950-1:2006: Information technology equipment — Safety — Part 1: General requirements.

ATS9360 also follows the provisions of the following directives: 2006/95/EC (Low Voltage Equipment); 2004/108/EC (Electromagnetic Compatibility).

FCC & ICES-003 Compliance

ATS9360 has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15, subpart B of the FCC Rules, and the Canadian Interference-Causing Equipment Standard ICES-003:2004.

ATS9360

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System Requirements

Personal computer with at least one free x8 or x16 PCI Express slot (must be Gen 2 or Gen 3 slot to achieve full data throughput), 4 GB RAM, 100 MB of free hard disk space, SVGA display adaptor and monitor with at least a 1024 x 768 resolution.

Power Requirements

+12 V	2.0 A, typical
+3.3 V	1.25 A, typical

Physical

Size	Single slot, half length PCI Express card (4.377 inches x 6.5 inches excluding the connectors protruding from the front panel)
Weight	250 g

I/O Connectors

ECLK, CH A, CH B, TRIG IN, AUX I/O	SMA female connector

Environmental

Operating temperature	0 to 55 degrees Celsius
Storage temperature	-20 to 70 degrees Celsius
Relative humidity	5 to 95%, non-condensing

Acquisition System

Resolution	12 bits
Bandwidth (-3 dB)	
DC-coupled, 50 Ω	DC - 800 MHz
Number of channels	2, simultaneously sampled
Maximum sample rate	1.8 GS/s single shot
Minimum sample rate	1 KS/s single shot for internal clocking
Full scale input ranges	
50 Ω input impedance:	±400 mV
DC accuracy	±2% of full scale in all ranges
Input coupling	DC
Input impedance	50 Ω ±1%
Input protection	
50 Ω	±4 V (DC + peak AC for CH A, CH B and EXT only without external attenuation)

Acquisition Memory System

Memory size	8 GB (4 Gigasamples in one channel mode)
Record length	Software-selectable with 128-point resolution. Record length must be a minimum of 256 points. There is no upper limit on the maximum record length.
Number of records	Software selectable from a minimum of 1 to a maximum of infinite number of records
Pre-trigger depth	From 0 to 8176 for single channel From 0 to 4088 for dual channel
Post-trigger depth	Record Length – Pre-Trigger Depth

Timebase System

Timebase options	Internal Clock or External Clock (Optional)
Internal sample rates	1.8 GS/s, 1.5 GS/s, 1.2 GS/s, 1 GS/s, 800 MS/s, 500 MS/s, 200 MS/s, 100 MS/s, 50 MS/s, 20 MS/s, 10 MS/s, 5 MS/s, 2 MS/s, 1 MS/s
Internal clock accuracy	±2 ppm

Dynamic Parameters

Typical values measured on the 200 mV range of CH A of a randomly selected ATS9360. Input signal was provided by an SRS SG384 signal generator, followed by a 9-pole, 10 MHz band-pass filter (TTE Q36T-10M-1M-50-720BMF). Input frequency was set at 9.9 MHz and output amplitude was 135 mV rms, which was approximately 95% of the full scale input. Input was averaged.

SNR	57.1 dB
SINAD	56.6 dB

Note that these dynamic parameters may vary from one unit to another, with input frequency and with the full scale input range selected.

Optional ECLK (External Clock) Input

Signal level	500 mV_{P-P} to 2 V_{P-P}
Input impedance	50 Ω
Input coupling	AC
Maximum frequency for Fast External Clock	1.8 GHz
Minimum frequency for Fast External Clock	300 MHz 75 MHz for Screened ECLK boards
Sampling edge	Rising only

Optional 10 MHz Reference PLL Input

Signal level	400 mV_{P-P} to 2 V_{P-P}
Input impedance	50 Ω
Input coupling	AC coupled
Input frequency	10 MHz ± 0.1 MHz
Maximum frequency	10.1 MHz
Minimum frequency	9.9 MHz
Sampling clock frequency	Any multiple of 1 MHz between 300 MHz and 1.8 GHz

Triggering System

Mode	Edge triggering with hysteresis
Comparator type	Digital comparators for internal (CH A, CH B) triggering and analog comparators for TRIG IN (External) triggering
Number of trigger engines	2
Trigger engine combination	Engine J, engine K, J OR K, software selectable
Trigger engine source	CH A, CH B, EXT, Software or None, independently software selectable for each of the two Trigger Engines
Hysteresis	±5% of full scale input, typical

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Trigger sensitivity	±10% of full scale input range. This implies that the trigger system may not trigger reliably if the input has an amplitude less than ±10% of full scale input range selected
Trigger level accuracy	±5%, typical, of full scale input range of the selected trigger source
Bandwidth	250 MHz
Trigger delay	Software selectable from 0 to 9,999,999 sampling clock cycles
Trigger timeout	Software selectable with a 10 µs resolution. Maximum settable value is 3,600 seconds. Can also be disabled to wait indefinitely for a trigger event

TRIG IN (External Trigger) Input

Input type	Analog or 3.3 V TTL (5 V compliant), software selectable
Input coupling	DC only
Analog input impedance	50 Ω
Analog bandwidth (-3 dB)	DC - 250 MHz
Analog input range	±2.5 V
Analog DC accuracy	±10% of full scale input
Analog input protection	±8 V (DC + peak AC without external attenuation)
TTL input impedance	6.7 kΩ ±10%
TTL min. pulse width	32 ADC sampling clocks
TTL min. pulse amplitude	2 Volts
TTL input protection	-0.7 V to + 5.5 V

Auxiliary I/O (AUX I/O)

Signal direction	Input or Output, software-selectable. Trigger Output by default
Output types:	Trigger Output, Pacer (programmable clock) Output, Software-controlled Digital Output
Input types:	Trigger Enable Software-readable Digital Input
Output	
Amplitude:	5 Volt TTL
Synchronization:	Synchronized to a clock derived from the ADC sampling clock. Divide-by-4 clock (dual channel mode) or divide-by-8 clock (single channel mode)
Input	
Amplitude:	3.3 Volt TTL (5 Volt-compliant)

Materials Supplied

ATS9360 PCI Express Card
ATS9360 Install Disk on USB flash drive

Certification and Compliances

RoHS 3 (Directive 2015/863/EU) Compliance
CE Marking — EC Conformity
FCC Part 15 Class A / ICES-003 Class A Compliance

All specifications are subject to change without notice

ORDERING INFORMATION

ATS9360-4G	ATS9360-101
ATS9360: External Clock Upgrade	ATS9360-005
ATS9360: Screened Ext Clk Upgrade	ATS9360-006
ATS9360-4G: One Year Extended Warranty	ATS9360-061
Software Development Kit 1 Year Subscription (Supports C/C++, Python, MATLAB, and LabVIEW)	ATS-SDK
ATS-GPU-BASE: GPU Streaming Library 1 Year Subscription	ATSGPU-001
ATS-GPU-OCT: Signal Processing Library 1 Year Subscription (requires ATSGPU-001)	ATSGPU-101

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DATASHEET REVISION HISTORY

Changes from version 1.6F (May 2019) to version 1.6G

	Section, Page
Changed *Sampling Rate* column to *Max. Sample Rate*	Feature Table, pg. 1
Added AlazarFrontPanel (for Linux) as benchmarking tool	Maximum Sustained Transfer Rate, pg. 2
Replaced signal sine or square wave requirement with high slew rate Because signal levels differ for Fast External Clock and 10 MHz Reference Clock, replaced min. and max. amplitude with a note that signal levels specified on page 7 must be respected.	Optional External Clock, pg. 5
Removed qualified metrology lab as option for recalibrating ATS9360	Calibration, pg. 5
Specified Windows 7 version support, re-ordered list of operating systems, and added end-of-support notice for Windows 7 and Windows Server 2008 R2	Support for Windows, pg. 5
Specified Linux distributions: CentOS, Debian, and Ubuntu	Linux Support, pg. 6
Updated handbook name and date: Export and brokering controls handbook, amended August 2019	Export Control Classification, pg. 6
Changed signal level from "400 mV_{P-P} to 1.6 V_{P-P}" to "500 mV_{P-P} to 2 V_{P-P}" Removed sine or square wave requirement for signal level Removed maximum amplitude, information included in signal level	Optional ECLK (External Clock) Input, pg. 7
Changed signal level from ±200 mV to "400 mV_{P-P} to 2 V_{P-P}" Removed sine or square wave requirement for signal level	Optional 10 MHz Reference PLL Input, pg. 7
Corrected Output types (removed Busy Output and added Pacer Output)	Auxiliary I/O (AUX I/O), pg. 8

Changes from version 1.6E (Nov 2018) to version 1.6F

	Section, Page
Updated ATS-GPU data transfer rate and benchmarks (FFTs per second, number of channels, and GPU)	ATS-GPU, pg. 5
Removed *ATS-GMA* section as this product is being discontinued	ATS-GMA, pg. 6
Added section *Extended Warranty*	Extended Warranty, pg. 6
Updated effective date of the new Export Control Handbook (May 17, 2019)	Export Control Classification, pg. 6
Removed ATS-GMA order numbers (ATSGMA-001, ATSGMA-101)	Ordering Information, pg. 8
Updated Trademark information	pg. 8

Changes from version 1.6D (Sept 2018) to version 1.6E

	Section, Page
Updated Power Requirements for both +12 V and +3.3 V	Power Requirements, pg. 8

Changes from version 1.6C (Jan 2018) to version 1.6D

	Section, Page
Updated RoHS Compliance to RoHS 3	Global change
Clarified Operating System Support	Feature Table, pg. 1
Updated *Recommended Motherboards or PCs*	Recommended Motherboards or PCs, pg. 2
Correction of trigger engines: changed to J and K (instead of X and Y)	Triggering, pg. 4
Specified that *External Trigger Input* 3.3 V TTL input is 5 V-compliant, and added note about LSB being replaced by the state of the external trigger signal source	External Trigger Input, pg. 4
Added information on ATS-SDK license	Software Development Kits, pg. 5
Specified 64-bit version for Windows and Linux support	ATS-GPU, pg. 5
Added *ATS-GMA* section	ATS-GMA, pg. 6
Added list of supported Microsoft Windows versions	Support for Windows, pg. 6
Added *Acquisition Memory System* section	Acquisition Memory System, pg. 8
Clarified that Max. and Min. Frequencies are for Fast External Clock, and added Maximum Amplitude: 2 V_{P-P}	Optional ECLK (External Clock) Input, pg. 8
Added "PLL" to section name for clarity, corrected Input Frequency tolerance, and added Max. and Min. Frequencies	Optional 10 MHz Reference PLL Input, pg. 8
Corrected Trigger Engine Combination	Triggering System, pg. 8
Clarified specs by providing separate specifications for Analog and TTL input, Added TTL min. pulse width, TTL min. pulse amplitude, and TTL input protection	TRIG IN (External Trigger) Input, pg. 9
Replaced TRIG OUT Output section with Auxiliary I/O (AUX I/O), and	Auxiliary I/O (AUX I/O), pg. 9
Added subscription length for ATS-SDK, ATSGPU-001, ATSGPU-101, and added products ATSGMA-001, ATSGMA-101	Ordering Information, pg. 9
Added Trademark information	pg. 9

DATASHEET REVISION HISTORY

Changes from version 1.6B (Oct 2017) to version 1.6C	Section, Page
Updated and moved section on FPGA-based FFT from page 4	FPGA-based FFT Processing, pg. 3
Added NPT AutoDMA buffer footer name	No Pre-Trigger (NPT) AutoDMA, pg. 3
Added section on Data Packing Mode	Data Packing Mode, pg. 3
Added section on OCT Ignore Bad Clock	OCT Ignore Bad Clock, pg. 4
Added note about Trigger Enable Input use in OCT	AUX Connector, pg. 5
Added CNRC as calibration standard	Calibration, pg. 5
Added -BASE and -OCT to ATS-GPU description for clarity	ATS-GPU, pg. 5
Corrected size of card	Physical, pg. 7
Updated email address	Manufactured By, pg. 8

Changes from version 1.6A (Sept 2017) to version 1.6B	Section, Page
Updated description for product ATSGPU-001 & ATSGPU-101	Ordering Information System, pg. 8

Changes from version 1.6 (July 2017) to version 1.6A	Section, Page
Specified conditions for obtaining a Linux driver source code license	Linux Support, pg. 5
Added Export Control Classification information	Export Control Classification, pg. 5
Removed product ATS9360-LINUX	Ordering Information System, pg. 8
Added product ATS9360-061	Ordering Information System, pg. 8
Replaced product ATSGPU-1YR with ATSGPU-001	Ordering Information System, pg. 8
Updated description for product ATSGPU-101	Ordering Information System, pg. 8

Changes from version 1.3 (Aug. 2015) to version 1.6	Section, Page
Added Python to list of supported languages for Software Development Kit	Features, pg. 1
Corrected FFT length for FPGA-based FFT (4096-point FFT instead of 2048)	Overview, pg. 1
Added Python & LabVIEW to list of supported languages for ATS-SDK, removed ATS-VI	Overview, pg. 1
Removed 1 GHz bandwidth option	Analog Input, pg. 2
Corrected FFT length for FPGA-based FFT (4096-point FFT instead of 2048)	FPGA Based FFT Processing, pg. 3
Removed *GPU Based FFT Processing or Other DSP*, integrated with ATS-GPU	GPU Based FFT Processing or Other DSP, pg. 4
Updated Input Impedance for TTL input to 6.7 kΩ	External Trigger Input, pg. 4
Modified AlazarDSO description	AlazarDSO Software, pg. 5
Updated ATS-SDK description	Software Development Kits, pg. 5
Updated ATS-GPU description	ATS-GPU, pg. 5
Added new Linux driver information and download link, updated description	Support for Linux, pg. 5
Added section on RoHS compliance	RoHS Compliance, pg. 5
Added section on EC Conformity	EC Conformity, pg. 5
Added section on FCC & ICES-003 Compliance	FCC & ICES-003 Compliance, pg. 5
Updated External Trigger Input Impedance for TTL input to 6.7 kΩ ±10%	TRIG IN (External Trigger) Input, pg. 7
Updated list of Certification and Compliances	Certification and Compliances, pg. 7
Removed products ATS9360-007, ATS9360-008, ATSGPU-WIN	Ordering Information, pg. 7
Corrected order number for ATS9360-LINUX	Ordering Information, pg. 7
Added products ATSGPU-1YR, ATSGPU-101	Ordering Information, pg. 7