ATS9625

250 MS/s 16-Bit AC-coupled PCIe Digitizer

- 2 channels sampled at 16-bit resolution
- 250 MS/s real-time sampling rate
- 75 dB Signal To Noise Ratio
- PCI Express (8-lane) interface
- 2 Gigasamples on-board dual-port memory
- Continuous streaming mode
- Asynchronous DMA device driver
- AlazarDSO® oscilloscope software
- Software Development Kit supports C/C++, C#, Python, MATLAB®, LabVIEW®
- Support for Windows® & Linux®

RoHS 3 COMPLIANT
2015/863/EU

CE

For new designs, please use ATS9428 or ATS9628

Product	Bus	Operating System	Channels	Max. Sample Rate	Bandwidth	Memory Per Channel	Resolution
ATS9625	PCIe x8	64-bit Windows & 64-bit Linux	2	250 MS/s	1 ~ 150 MHz Optional 250 MHz	Up to 2 Gigasamples	16 bits

Overview

AlazarTech ATS®9625 is an 8-lane PCI Express (PCIe x8), dual-channel, high-speed, 16-bit, 250 MS/s waveform digitizer card capable of streaming acquired data to PC memory at rates up to 1.6 GB/s or storing it in its deep on-board dual-port acquisition memory buffer of up to 2 Gigasamples.

The on-board Coprocessor FPGA is an Altera Stratix III device with on-chip memory, hardware multipliers, DSP blocks and a fast fabric that allows both integer based and floating-point digital signal processing.

All data acquired by the on-board A/D converters flows through the Coprocessor FPGA.

The main difference between ATS9626 and ATS9625 is input coupling: ATS9626 provides dc coupling, whereas ATS9625 provides ac coupling.

ATS9625 is supplied with AlazarDSO software that lets the user get started immediately without having to go through a software development process.

Users who need to integrate the ATS9625 in their own program can purchase a software development kit, ATS-SDK, for C/C++, C#, Python, MATLAB, and LabVIEW for both Windows and Linux operating systems.

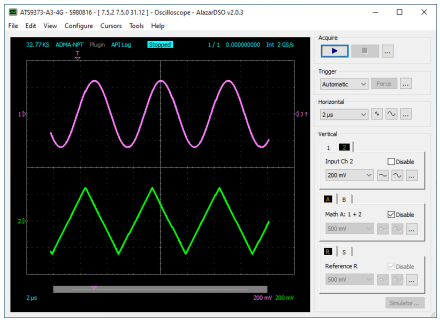
All of this advanced functionality is packaged in a low power, half-length PCI Express card.

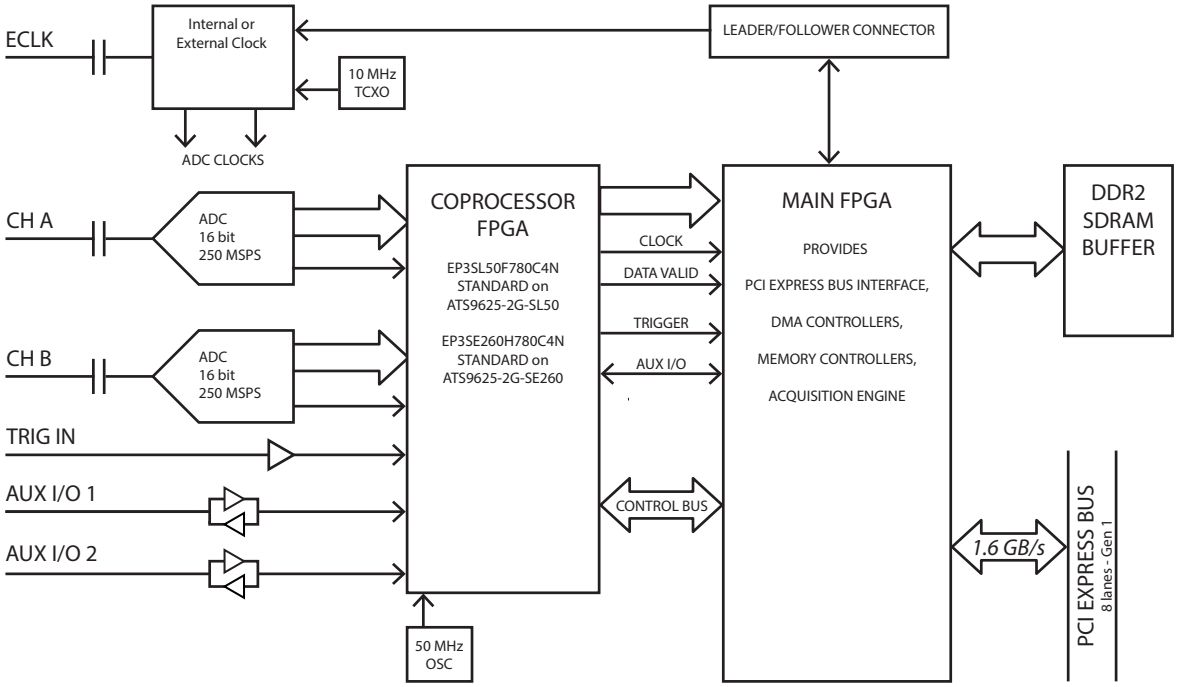
Applications

Optical Coherence Tomography (OCT)
Radar/RF Signal Recording & Analysis
Ultrasonic & Eddy Current NDT/NDE
Terabyte Storage Oscilloscope
High Resolution Oscilloscope
Lidar
Spectroscopy
Digital Down Conversion (DDC)
Multi-Channel Transient Recording

Please note: It is no longer possible for users to design their own Coprocessor FPGA.

We have discontinued the ATS962x Coprocessor FPGA Development Kit (also called ATS9625-FDK) due to lack of demand.





PCI Express Bus Interface

ATS9625 interfaces to the host computer using an 8-lane PCI Express bus. Each lane operates at 2.5 Gbps.

According to PCIe specification, an 8-lane board can be plugged into any 8-lane or 16-lane slot, but not into a 4-lane or 1-lane slot. As such, ATS9625 requires at least one free 8-lane or 16-lane slot on the motherboard.

The physical and logical PCIe x8 interface is provided by an on-board FPGA, which also integrates acquisition control functions, memory management functions and interface to Coprocessor FPGA. This very high degree of integration maximizes product reliability.

The AlazarTech® bus benchmark has been proven on many computers, including workstation and server class machines from Dell™ and HP, as well as no-name machines built around motherboards from Intel®, ASUS®, TYAN®, Supermicro®, etc.

Users must always be wary of throughput specifications from manufacturers of waveform digitizers. Some unscrupulous manufacturers tend to specify the raw, burst-mode throughput of the bus. Others mention data throughput rates to operating system kernel memory, not user accessible memory.

AlazarTech, on the other hand, specifies the benchmarked sustained throughput to buffers in user space.

To achieve such high throughput, a great deal of proprietary memory management logic and kernel mode drivers have been designed by AlazarTech.

Analog Input

An ATS9625 has two transformer coupled analog input channels. Each channel has analog input bandwidth from 1 MHz to 150 MHz.

The full scale input range is fixed at 2.5 V_{P-P} calibrated at 10 MHz input signal.

Input impedance of both channels is fixed at 50 Ω. It must be noted that this impedance is dynamic in nature and not resistive.

Acquisition System

ATS9625 PCI Express digitizers use state of the art 250 MSPS, 16-bit ADCs to digitize the input signals. The real-time sampling rate of the ADCs ranges from 250 MS/s down to 50 MS/s.

The two channels are guaranteed to be simultaneous, with a maximum clock skew of 10 ps. Additive jitter of the clock distributor circuit is less than 225 fs_{rms}.

An acquisition can consist of multiple records, with each record being captured as a result of one trigger event. A record can contain both pre-trigger and post-trigger data.

Infinite number of triggers can be captured by ATS9625, when it is operating using dual-port memory.

In between the multiple triggers being captured, the acquisition system is re-armed by the hardware within 256 sampling clock cycles.

This mode of capture, sometimes referred to as Multiple Record, is very useful for capturing data in applications with a very rapid or unpredictable trigger rate. Examples of such applications include medical imaging, ultrasonic testing, OCT and NMR spectroscopy.

Coprocessor FPGA

ADC data flows through the Coprocessor FPGA before it is stored in the on-board memory or transferred to host PC memory.

Note: it is no longer possible for users to design their own Coprocessor FPGA. The ATS962x Coprocessor FPGA Development Kit has been discontinued.

On-Board Acquisition Memory

ATS9625 features an on-board dual-ported memory buffers of 2 Gigasamples.

Acquisition memory can either be divided equally between the two input channels or devoted entirely to one of the channels.

The main advantage of having on-board memory is that it acts as a very deep FIFO between the Analog-to-Digital converters and PCI Express bus, allowing very fast sustained data transfers across the bus, even if the operating system or another motherboard resource temporarily interrupts DMA transfers.

High-Capacity Coprocessor FPGA

The ATS9625-2G-SL50 digitizer includes an Altera Stratix III EP3SL50F780C4N device for the Coprocessor FPGA. For some users, this FPGA may not have enough resources to implement their entire design.

In such situations, users can order ATS9625-2G-SE260 to have the high-capacity EP3SE260H780C4N Coprocessor FPGA. Note that orders for high capacity FPGA may have a significant lead-time.

Maximum Sustained Transfer Rate

PCI Express support on different motherboards is not always the same, resulting in significantly different sustained data transfer rates. The reasons behind these differences are complex and varied and will not be discussed here.

ATS9625 users can quickly determine the maximum sustained transfer rate for their motherboard by inserting their card in a PCIe slot and running the bus benchmarking tool provided in AlazarDSO for Windows or AlazarFrontPanel for Linux.

ATS9625, which is equipped with dual-port on-board memory, will be able to achieve this maximum sustained transfer rate.

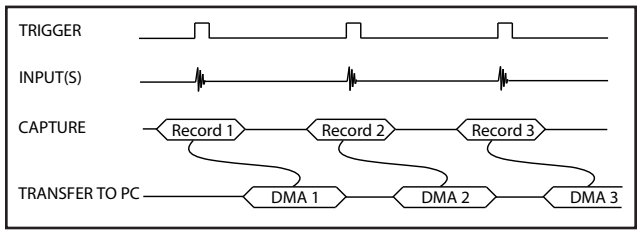
Recommended Motherboards or PCs

Many different types of motherboards and PCs have been benchmarked by AlazarTech. The ones that have produced the best throughput results (as high as 1.7 GB/s for PCIe Gen 1) are listed here: www.alazartech.com/images-media/2246-AlazarTechRecommendedMotherboards.pdf.

It should be noted that some motherboards may behave unexpectedly. For example, one customer purchased a P6T6 motherboard (instead of P6T7) and found that the throughput was limited to approximately 800 MB/s because P6T6 only supports 4-lane PCI Express connection, even though it uses the same x58 chipset.

Traditional AutoDMA

In order to acquire both pre-trigger and post-trigger data in a dual-ported memory environment, users can use Traditional AutoDMA.



Data is returned to the user in buffers, where each buffer can contain from 1 to 8191 records (triggers). This number is called RecordsPerBuffer.

Users can also specify that each record should come with its own header that contains a 40-bit trigger timestamp.

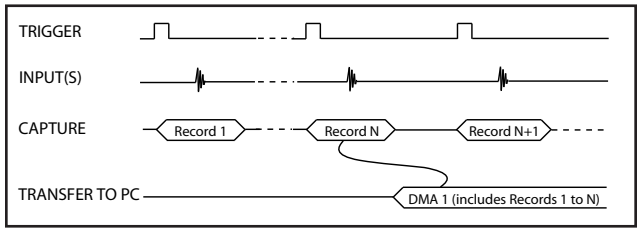
A BUFFER_OVERFLOW flag is asserted if more than 512 buffers have been acquired by the acquisition system, but not transferred to host PC memory by the AutoDMA engine.

In other words, a BUFFER_OVERFLOW can occur if more than 512 triggers occur in very rapid succession, even if all the on-board memory has not been used up.

No Pre-Trigger (NPT) AutoDMA

Many ultrasonic scanning and medical imaging applications do not need any pre-trigger data: only post-trigger data is sufficient.

NPT AutoDMA is designed specifically for these applications. By only storing post-trigger data, the memory bandwidth is optimized and the entire on-board memory acts like a very deep FIFO.



Note that a DMA is not started until RecordsPerBuffer number of records (triggers) have been acquired and written to the on-board memory.

NPT AutoDMA buffers do not include headers or footers.

More importantly, a BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up. This provides a very substantial improvement over Traditional AutoDMA.

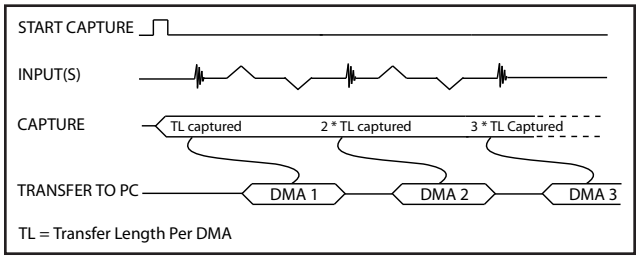
NPT AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow.

This is the recommended mode of operation for most ultrasonic scanning, OCT and medical imaging applications.

Continuous AutoDMA

Continuous AutoDMA is also known as the data streaming mode.

In this mode, data starts streaming across the PCIe bus as soon as the ATS9625 is armed for acquisition. It is important to note that triggering is disabled in this mode.



Continuous AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

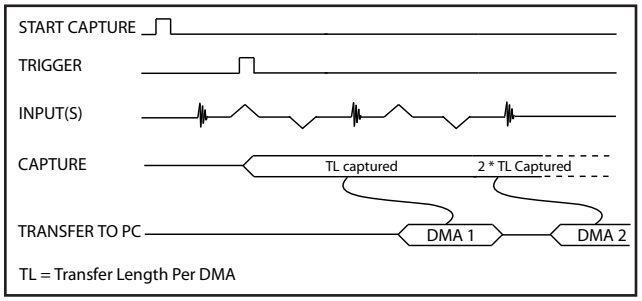
A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

The amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Continuous AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for very long signal recording.

Triggered Streaming AutoDMA

Triggered Streaming AutoDMA is virtually the same as Continuous mode, except the data transfer across the bus is held off until a trigger event has been detected.



Triggered Streaming AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

As in Continuous mode, the amount of data to be captured is controlled by counting the number of buffers acquired.

Acquisition is stopped by an AbortCapture command.

Triggered Streaming AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow.

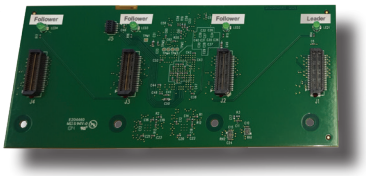
This is the recommended mode for RF signal recording that has to be started at a specific time, e.g. based on a GPS pulse.

Leader/Follower Systems

Users can create a multi-board Leader/Follower system by synchronizing up to four ATS9625 boards using an appropriate SyncBoard-9625.

SyncBoard-9625 is a mezzanine board that connects to the Leader/Follower connector along the top edge of the ATS9625 and sits parallel to the motherboard. For additional robustness, users can secure the SyncBoard-9625 to a bracket mounted on each of the ATS9625 boards.

SyncBoard-9625 is available is available in different widths: 2x, 4x, 2x-W, 3x-W or 4x-W.



SyncBoards with the -W suffix provide 2-slot spacing between ATS9625 cards to support some of the newer motherboards that space out the on-board x8 or x16 slots by two slots. The -W SyncBoards are also a better solution from thermal point of view, as there is better air flow with 2-slot spacing.

The 2x and 2x-W models allow 2-board Leader/Follower systems; the 3x-W model allows 2 or 3-board Leader/Follower systems; and the 4x and 4x-W models allow 2, 3 or 4 board Leader/Follower systems.

The Leader board's clock and trigger signals are copied by the SyncBoard-9625 and supplied to all the Follower boards. This guarantees complete synchronization between the Leader board and all Follower boards.

It should be noted that SyncBoard-9625 does not use a PLL-based clock buffer, allowing the use of variable frequency clocks in Leader/Follower configuration.

A Leader/Follower system samples all inputs simultaneously and also triggers simultaneously on the same clock edge.

Multi-board Systems using ATS 4X1G

ATS9625: Sync 4X1G is a device that allows simultaneous sampling across multiple independent ATS9625 waveform digitizers. This is achieved by providing common clock and trigger signals to each digitizer.

Sync 4X1G supports Trigger Enable and Trigger Disable so that users can delay triggering until all digitizers are armed; this is a distinct advantage over passive signal splitters.

ATS Sync 4X1G comes with a software library that allows user software to control it.

Sync 4X1G interfaces to AlazarTech digitizer cards using a proprietary high-frequency cable. The provided cable terminates in a ganged micro-miniature RF connector, which is used to connect to the Sync 4X1G.

The other end of the cable terminates in male SMA and BNC connectors, which are used to connect to the digitizer External Clock and External Trigger respectively.

Sync 4X1G connects to the host computer using a provided USB cable. Please refer to the ATS Sync 4X1G datasheet for full specifications.

Asynchronous DMA Driver

The various AutoDMA schemes discussed above provide hardware support for optimal data transfer. However, a corresponding high performance software mechanism is also required to make sure sustained data transfer can be achieved.

This proprietary software mechanism is called Async DMA (short for Asynchronous DMA).

A number of data buffers are posted by the application software. Once a data buffer is filled, i.e. a DMA has been completed, ATS9625 hardware generates an interrupt, causing an event message to be sent to the application so it can start consuming data. Once the data has been consumed, the application can post the data buffer back on the queue. This can go on indefinitely.

One of the great advantages of Async DMA is that almost 95% of CPU cycles are available for data processing, as all DMA arming is done on an event-driven basis.

To the best of our knowledge, no other supplier of waveform digitizers provides asynchronous software drivers. Their synchronous drivers force the CPU to manage data acquisition, thereby slowing down the overall data acquisition process.

Output Data Format

By default, ATS9625 data comes out as unsigned binary, where code 0 represents the negative full scale, code (2^n-1) represents the positive full scale with zero being 2^{n-1}.

It is possible to change the data format to signed binary using an API call. In signed binary format, zero is represented by code 0, positive full scale is represented by (2^{n-1}-1) and negative full scale is represented by (2^{n-1}).

Wideband Input Upgrade

A Wideband Input Upgrade (order number ATS9625-012) can be purchased. Bandwidth can be extended to 250 MHz with minimal effect on noise performance.

Triggering

ATS9625 is equipped with sophisticated digital triggering options, such as programmable trigger thresholds and slope on any of the input channels or the External Trigger input.

Coprocessor FPGA has access to external trigger and two auxiliary I/O signals.

While most oscilloscopes offer only one trigger engine, ATS9625 offers two trigger engines (called Engines J and K).

The user can specify the number of records to capture in an acquisition, the length of each record and the amount of pre-trigger data.

A programmable trigger delay can also be set by the user. This is very useful for capturing the signal of interest in a pulse-echo application, such as ultrasound, radar, lidar etc.

External Trigger Input

The external trigger input on the ATS9625 is labeled TRIG IN on the face plate.

External Trigger must an LVTTL digital signal, i.e. 0 to 3.3 V TTL signal. Minimum pulse height requirement is 2.0 Volts. Input impedance of this input is 6.4 kΩ.

Analog signals and smaller amplitude digital signals will not be detected as trigger events.

User can select between rising edge and falling edge of this signal as the trigger event.

It should be noted that the TRIG IN signal passes through the Coprocessor FPGA. This description of TRIG IN applies to the default Coprocessor FPGA shipped with ATS9625 drivers. A custom Coprocessor FPGA can completely change the functionality of this signal.

Timebase

ATS9625 timebase can be controlled either by on-board low-jitter VCO or by External Clock.

On-board low-jitter VCO uses an on-board 10 MHz TCXO as a reference clock.

External Clock

While the ATS9625 features low-jitter VCO and a 10 MHz TCXO as the source of the timebase system, there may be occasions when digitizing has to be synchronized to an external clock source.

ATS9625 includes an SMA input for an external clock signal, which should be a high slew rate signal or 1.6 V digital signal.

Input impedance for the External Clock input is fixed at 50 Ω. External clock input is always AC-coupled.

There are two types of External Clock supported by ATS9625. These are described below.

Fast External Clock

A new sample is taken by the on-board ADCs for each rising edge of this External Clock signal.

In order to satisfy the clocking requirements of the ADC chips being used, Fast External Clock frequency must always be higher than 50 MHz and lower than 250 MHz.

This is the ideal clocking scheme for OCT applications.

10 MHz Reference Clock

It is possible to generate the sampling clock based on an external 10 MHz reference input. This is useful for RF systems that use a common 10 MHz reference clock.

ATS9625 uses an on-board low-jitter VCO to generate the 250 MHz high frequency clock used by the ADC. This 250 MS/s sampled data can then be decimated by a factor of 1 to 100000.

Dummy Clock Switchover

OCT applications require interfacing the ATS9625 to a variable clock frequency (called k-clock) from a swept-source laser.

In most cases, k-clock frequency can be out of specification for a short period of time, i.e. the frequency is slower than 50 MHz for a short period of time.

ATS9625 has a built-in Dummy Clock generator and a clock switchover mechanism that can be used to avoid operating the A/D chips outside of their specifications.

This unique feature of the ATS9625 can be the difference between a fully working OCT system and one that cannot provide reliable data.

AUX Connectors

ATS9625 provides two AUX (Auxiliary) SMA connectors that can be used for interfacing to external digital signals.

AUX 1 can be configured as either an Input or Output. It is configured as a Trigger Output by default.

AUX 2 is a Trigger Output.

When configured as a Trigger Output, AUX SMA connector outputs a 5 Volt TTL signal synchronous to the ATS9625 Trigger signal, allowing users to synchronize their test systems to the ATS9625 Trigger.

When combined with the Trigger Delay feature of the ATS9625, this option is ideal for ultrasonic and other pulse-echo imaging applications.

AUX connector can also be used as a Trigger Enable Input and Clock Output.

Another application for AUX connector is that users can input the 1 PPS pulse from a GPS receiver into the ATS9625 (and the Coprocessor FPGA).

Calibration

Every ATS9625 digitizer is factory calibrated to NIST- or CNRC-traceable standards. To recalibrate an ATS9625, the digitizer must be shipped back to the factory.

AlazarDSO Software

ATS9625 is supplied with the powerful AlazarDSO software that allows the user to setup the acquisition hardware and capture, display and archive the signals.

The Stream-To-Memory command in AlazarDSO allows users to stream a large dataset to motherboard memory.

AlazarDSO software also includes powerful tools for benchmarking the computer bus and disk drive.

Software Development Kits

AlazarTech provides easy-to-use software development kits for customers who want to integrate the ATS9625 into their own software.

A Windows-compatible software development kit, called ATS-SDK, includes headers, libraries and source code sample programs written in C/C++, C#, Python, MATLAB, and LabVIEW.

A Linux-compatible software development kit, called ATS-devel, includes headers, libraries and source code sample programs written in C++ and Python.

These programs can fully control the ATS9625 and acquire data in user buffers.

The purchase of an ATS-SDK license includes a subscription that allows users to download ATS-SDK updates from the AlazarTech website for period of 12 months from the date of purchase.

Customers who want to download new releases beyond this 12 month period should purchase extended maintenance (order number ATS-SDK-1YR).

ATS-GPU

ATS-GPU is a software library developed by AlazarTech to allow users to do real-time data transfer from ATS9625 to a GPU card at rates up to 1.6 GB/s.

Interfacing waveform digitizers to GPUs involves creating a software mechanism to move data from one to the other and back to user buffers. The standard techniques used most often can get the job done, but feature very low data throughput due to software overheads.

AlazarTech designed ATS-GPU to eliminate this software bottleneck so that data can be moved from AlazarTech digitizers to GPUs and from GPUs to user buffers at full PCIe bus speeds. Once the data is

available in GPU memory, many types of digital signal processing (DSP) can be done on this data at near-hardware speeds.

ATS-GPU-BASE is supplied with an example user application in source code. The application includes GPU kernels that use ATS-GPU to receive data, do very simple signal processing (data inversion), and copy the processed (inverted) data back to a user buffer. All this is done at the highest possible data transfer rate.

Programmers can replace the data inversion code with application-specific signal processing kernels to develop custom applications.

Version 23.1.0 and higher of ATS-GPU-BASE includes a Boxcar Averaging example kernel that provides the ability to perform real-time boxcar averaging on signals acquired by AlazarTech waveform digitizers. It uses optimized GPU routines that allow raw data acquisition rates up to 6.9 GB/s. This signal processing module can lead to a major improvement of signal-to-noise ratio without using CPU resources and without doing FPGA programming.

ATS-GPU-OCT is the optional OCT Signal Processing library for ATS-GPU. It contains floating-point FFT routines that have also been optimized to provide the maximum number of FFTs per second. Kernel code running on the GPU can do zero-padding, apply a windowing function, do a floating-point FFT, calculate the amplitude and convert the result to a log scale. It is also possible to output phase information.

FFTs can be done on triggered data or on continuous gapless stream of data. It is also possible to do spectral averaging. Our benchmarks showed that it was possible to do 240,000 FFTs per second when capturing data in dual-channel mode and using a NVIDIA® Quadro® P5000 GPU.

ATS-GPU-NUFFT is an extension of ATS-GPU-OCT that allows non-uniform FFTs to be performed on data acquired uniformly in time domain using a fixed sampling rate. For SS-OCTs where the wavelength does not vary linearly in time, a fixed sampling rate results in data that is non-uniformly distributed in frequency domain. ATS-GPU-NUFFT allows linearized FFTs to be performed on such data.

ATS-GPU supports 64-bit Windows and 64-bit Linux for CUDA®-based development.

Support for Windows

Windows support for ATS9625 includes Windows 11, Windows 10, Windows Server® 2019, and Windows Server 2016. As Windows Server 2019 and 2016 are seldom used by our customers, they are expected to work but are not regularly tested with each software release. If there are issues related to Windows Server 2016 or 2019, tech support may not be as rapid as for other operating systems.

Only 64-bit Windows operating systems are supported. The last 32-bit Windows driver is version 5.10.24, which supports Windows 7.

Microsoft mainstream support ended in 2018 for Windows 8.1 and Windows Server 2012 R2. As such, AlazarTech has ceased development on these operating systems. Current software and driver releases may work with these operating systems but they are not officially supported.

Due to lack of demand and due to the fact that Microsoft no longer supports these operating systems, AlazarTech no longer supports Windows 8, Windows 7, Windows XP, Windows Vista, Windows Server 2012, Windows Server 2008 R2, and Windows Server 2008.

Linux Support

AlazarTech offers Dynamic Kernel Module Support (DKMS) drivers for the following Linux distributions: Ubuntu, Debian, and RHEL®.

AlazarTech DKMS drivers may work for other Linux distributions but they have not been tested and technical support may be limited.

Users can download the DKMS driver and associated library for their specific distribution here:
www.alazartech.com/en/linux-drivers/ats9625/11/

Only 64-bit Linux operating systems are supported.

A GUI application called AlazarFrontPanel that allows simple data acquisition and display is also provided.

ATS-SDK includes source code example programs for Linux, which demonstrate how to acquire data programmatically using a C compiler. Note that example programs are only provided for Python and C++.

Based on a minimum annual business commitment, the Linux driver source code license (order number ATS9625-LINUX) may be granted to qualified OEM customers for a fee. For release of driver source code, a Non-Disclosure Agreement must be executed between the customer's organization and AlazarTech.

All such source code disclosures are made on an as-is basis with limited support from the factory.

Accessories for Out-of-Warranty Products

Accessories, such as SyncBoards, purchased for use with in-warranty digitizer cards will be covered by a 1-year warranty.

Accessories purchased for use with out-of-warranty digitizers will not be warranted against defects in materials and workmanship. As AlazarTech cannot verify with certainty that the cause of any malfunction is not due to the non-warranted digitizer, accessories purchased for out-of-warranty digitizers will require a warranty waiver.

Upgrading Your Digitizer in The Field

It is always recommended to get upgrades installed at the factory with the initial digitizer purchase.

If the digitizer is still under warranty, it may be possible to add certain upgrades in the field, but there is a small chance that the upgrade will not work, in which case the digitizer would need to be returned to the factory to complete the upgrade.

If the digitizer is no longer under warranty, the upgrade must be done at the factory and there will be a minimum service charge in addition to the cost of the upgrade. This is so that AlazarTech can verify that the digitizer meets basic performance levels prior to any upgrade.

Technical Support

AlazarTech is known for its world-class technical support. Customers receive free technical support on hardware products that are under warranty.

AlazarTech digitizers come with a standard one (1) year parts and labor warranty. This warranty can be extended for a fee (more information can be found in the *Extended Warranty* section below).

If your waveform digitizer is out of warranty, you will not be eligible for free technical support on AlazarTech hardware or software products and you will need to purchase technical support hours (order number SUPPORT-HR5) to obtain assistance.

In addition, any necessary repairs to your out-of-warranty hardware products will carry a minimum bench charge.

Extended Warranty

The purchase of an ATS9625 includes a standard one (1) year parts and labor warranty. AlazarTech hardware parts and labor warranty should be maintained to ensure uninterrupted access to technical support and warranty repair services.

Customers may extend their warranty by ordering the appropriate Extended Warranty (ATS9625-061 for ATS9625-SL50; ATS9625-062 for ATS9625-SE260). This should be purchased before expiration of the standard warranty (or before expiration of an Extended Warranty).

If the warranty lapses, renewal at a later date will be subject to a reinstatement fee, to cover the administrative costs of warranty reinstatement, and a 6-month waiting period for repair claims. Furthermore, warranty must be extended at least 6 months past the current date.

Users can purchase up to 4 (four) additional years of warranty extensions for a maximum total of 5 years of warranty.

Get your warranty end date by registering your product at: www.alazartech.com/en/my-account/my-products/.

Export Control Classification

According to the latest Export Control Handbook that came into effect on May 17, 2019, ATS9625 is classified by Export Controls Division of Government of Canada as a controlled product under ECL 1-3.A.2.h, which is equivalent to ECCN 3A002.h.

For sales where the ultimate country destination is Canada or U.S., no export permit is required unless the end-use of ATS9625, in part or in its entirety, is related to the development or deployment of weapons of mass destruction.

For shipments to eligible destinations, AlazarTech is allowed to export under a general export permit, unless the end-use of ATS9625, in part or in its entirety, is related to the development or deployment of weapons of mass destruction. For general export permit shipments, users must provide a signed export compliance statement (ECS) that includes a detailed description of the end-use. Shipments cannot be made without a signed ECS on file.

For all other countries, and for all cases where the end-use of ATS9625, in part or in its entirety, is related to the development or deployment of weapons of mass destruction, an export permit is required, which will require extensive details on the end-use and end-users. This process may cause significant delays.

RoHS Compliance

ATS9625 is fully RoHS compliant, as defined by Directive 2015/863/EU (RoHS 3) of the European Parliament and of the Council of 31 March 2015 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

All manufacturing is done using RoHS-compliant components and lead-free soldering.

REACH Compliance

AlazarTech verifies its supply chain against the latest REACH requirements. A compliance statement is usually available within 6 months of release of the European Chemicals Agency (ECHA) updated substance of very high concern (SVHC), Authorizations, and Restrictions lists.

EC Conformity

ATS9625 conforms to the following standards:

Electromagnetic Emissions:
CISPR 32:2015/AMD1:2019 /
EN 55032:2015/A11:2020 (Class A):
Multimedia Equipment (MME). Radio disturbance characteristics. Limits and method of measurement:
EN 61000-3-2:2014, EN 61000-3-3:2013.

Electromagnetic Immunity:
EN 55035:2017/A11:2020:
Multimedia Equipment (MME) Immunity characteristics — Limits and methods of measurement:
EN 61000-4-3:2006 + A1:2008 + A2:2010.

Safety:
IEC 62368-1:2014 / EN 62368-1:2014+A11:2017:
Audio/video, information and communication technology equipment - Part 1: Safety requirements.

ATS9625 also follows the provisions of the following directives: 2014/35/EU (Low Voltage Equipment); 2014/30/EU (Electromagnetic Compatibility).

FCC & ICES-003 Compliance

ATS9625 has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15, subpart B of the FCC Rules, and the Canadian Interference-Causing Equipment Standard ICES-003 issue 7 October 2020.

Processing Using Multiple CPU Cores

Programmers can take advantage of multiple cores available in modern CPUs to speed up signal processing.

Benchmarks have shown that a quad-core CPU can perform real-time averaging at a rate of 1.0 GB/s and only use up 20% of CPU cycles. Increasing the number of cores or decreasing the sample rate reduces CPU usage even further.

One of the main applications of using multiple cores to do signal processing is Quantum Computing and Spectroscopy applications, where each record contains partial information about the signal of interest and a large number of records must be accumulated to gather a representative dataset.

System Requirements

Personal computer with at least one free x8 or x16 PCI Express (v1.0a, v1.1 or v2.0) slot, 2 GB RAM, 100 MB of free hard disk space, SVGA display adaptor and monitor with at least a 1024 x 768 resolution.

Power Requirements

+12 V	2.0 A, typical
+3.3 V	2.0 A, typical

Physical

Size	Single slot, half length PCI Express card (4.377 inches x 6.5 inches excluding the connectors protruding from the front panel)
Weight	250 g

I/O Connectors

ECLK, CH A, CH B, TRIG IN, AUX I/O 1, AUX I/O 2	SMA female connectors

Environmental

Operating temperature	0 to 55 degrees Celsius, ambient
Storage temperature	-20 to 70 degrees Celsius
Relative humidity	5 to 95%, non-condensing

Acquisition System

Resolution	16 bits
Bandwidth (-3 dB)	
AC-coupled, 50 Ω	1 MHz - 150 MHz
Bandwidth with Wideband Upgrade	
AC-coupled, 50 Ω	1 MHz - 250 MHz
Number of channels	2, simultaneously sampled
Maximum Sample Rate	250 MS/s single shot
Minimum Sample Rate	1 KS/s single shot for internal clocking
Full Scale Input range:	2.5 V_{P-P} (calibrated at 10 MHz input)
Input coupling	AC only
Input impedance	50 Ω ±1%
Absolute maximum input	±4 V (DC + peak AC for CH A, CH B and TRIG IN only without external attenuation)

Acquisition Memory System

Memory size	128 MegaSamples, 1 GigaSamples or 2 GigaSamples
Record length	Software-selectable with 32-point resolution. Record length must be a minimum of 256 points. There is no upper limit on the maximum record length.
Number of records	Software-selectable from a minimum of 1 to a maximum of infinite number of records
Pre-trigger depth	From 0 to 4080 for single channel in NPT mode From 0 to 2040 for dual channel in NPT mode
Post-trigger depth	Record Length – Pre-Trigger Depth

Timebase System

Timebase options	Internal Clock or External Clock
Internal Sample Rates	250 MS/s, 125 MS/s, 100 MS/s, 50 MS/s, 20 MS/s, 10 MS/s, 5 MS/s, 2 MS/s, 1 MS/s, 500 KS/s, 200 KS/s, 100 KS/s, 50 KS/s, 20 KS/s, 10 KS/s, 5 KS/s, 2 KS/s, 1 KS/s
Internal Clock accuracy	±2 ppm

Dynamic Parameters

Typical values measured on CH A of a randomly selected ATS9625. Input signal was provided by a Marconi 2018A signal generator, followed by multi-pole band-pass filters (TTE Q36T family). Inputs were not averaged.

	5 MHz	10 MHz	20 MHz	50 MHz	100 MHz
SNR	75.29 dB	75.02 dB	75.04 dB	74.39 dB	71.67 dB
SINAD	74.47 dB	74.12 dB	74.24 dB	74.13 dB	70.72 dB
SFDR	91.60 dB	91.03 dB	90.87 dB	86.92 dB	79.95 dB
THD	-82.11 dB	-82.05 dB	-81.99 dB	-85.85 dB	-84.18 dB
ENOB	12.08	12.02	12.04	12.02	11.45

Fast External Clock Input

Connector	ECLK SMA connector
Signal Level	500 mV_{P-P} to 1.6 V_{P-P}
Input impedance	50 Ω
Input coupling	AC
Maximum frequency	250 MHz for Fast External Clock
Minimum frequency	50 MHz for Fast External Clock
Sampling Edge	Rising

Dummy Clock Switchover

Switchover mode	Available only when Fast External Clock is selected
Switchover start	Upon end of each record
Switchover time	Programmable with 5 ns resolution

10 MHz Reference PLL Input

Connector	ECLK SMA connector
Signal Level	500 mV_{P-P} to 1.6 V_{P-P}
Input impedance	50 Ω
Input Coupling	AC
Input frequency	10 MHz ± 0.1 MHz
Maximum frequency	10.1 MHz
Minimum frequency	9.9 MHz
Sampling Clock Freq.	250 MHz

Triggering System

Mode	Edge triggering with hysteresis
Comparator Type	Digital comparators for internal (CH A, CH B) triggering and analog comparators for TRIG IN (External) triggering
Number of Trigger Engines	2
Trigger Engine Combination	Engine J, engine K, J OR K, software-selectable

Trigger Engine Source	CH A, CH B, TRIG IN, Software or None, independently software-selectable for each of the two Trigger Engines
Hysteresis	±5% of full scale input, typical
Trigger sensitivity	±10% of full scale input range. This implies that the trigger system may not trigger reliably if the input has an amplitude less than ±10% of full scale input range selected
Trigger level accuracy	±5%, typical, of full scale input range of the selected trigger source
Bandwidth	50 MHz
Trigger Delay	Software-selectable from 0 to 9,999,999 sampling clock cycles
Trigger Timeout	Software-selectable with a 10 µs resolution. Maximum settable value is 3,600 seconds. Can also be disabled to wait indefinitely for a trigger event

TRIG IN (External Trigger) Input

Input type	Digital triggering (LVTTL)
Input impedance	6.4 kΩ ±10%
Coupling	DC only
Minimum pulse width	16 nanoseconds
Minimum pulse amplitude	2 Volt
Absolute maximum input	-0.7 V to +8 V

Auxiliary I/O (AUX 1)

Signal direction	Input or Output, software-selectable. Output by default
Output types:	Trigger Output, Pacer (programmable clock) Output, Software-controlled Digital Output
Input types:	Trigger Enable Software readable Digital Input
Output	
Amplitude:	5 Volt TTL
Synchronization:	Synchronized to a clock derived from the ADC sampling clock. Divide-by-4 clock (dual channel mode) or divide-by-8 clock (single channel mode)
Input	
Amplitude:	3.3 Volt TTL (5 Volt compliant)
Input coupling:	DC

TRIG OUT Output (AUX 2)

Connector Used	AUX 2
Output Signal	5 Volt TTL
Synchronization	Synchronized to a clock derived from the ADC sampling clock. Divide-by-4 clock (dual channel mode) or divide-by-8 clock (single channel mode)

Materials Supplied

ATS9625 PCI Express Card

ATS9625 Installation Disk (on USB Flash Drive)

Certification and Compliances

RoHS 3 (Directive 2015/863/EU) Compliance

REACH Compliance

CE Marking — EC Conformity

FCC Part 15 Class A / ICES-003 Class A Compliance

All specifications are subject to change without notice

ORDERING INFORMATION

ATS9625-SL50	ATS9625-002
ATS9625-SE260	ATS9625-003
SyncBoard-9625 2x	ATS9625-007
SyncBoard-9625 4x	ATS9625-008
ATS9625: Wideband Input Upgrade	ATS9625-012
ATS9625: SyncBoard 2x-W	ATS9625-020
ATS9625: SyncBoard 3x-W	ATS9625-021
ATS9625: SyncBoard 4x-W	ATS9625-022
ATS9625-SL50: One Year Extended Warranty	ATS9625-061
ATS9625-SE260: One Year Extended Warranty	ATS9625-062
ATS9625: Sync 4X1G	ATS9625-025
ATS Sync xX1G: AC Wall Adapter	SYNC-X1G-PWR
ATS Sync 4X1G: GRF1-SMA/BNC cable	SYNC-4X1-CBL
SYNC-4X1G: One Year Extended Warranty	SYNC-4X1-061
ATS-SDK purchased with a digitizer board or ATS-GPU: License + 1 Year Subscription (Supports C/C++, Python, MATLAB, and LabVIEW)	ATS-SDK
ATS-SDK purchased separately: License + 1 Year Subscription + 5 hours of technical support (Supports C/C++, Python, MATLAB, and LabVIEW)	ATS-SDK-WOD
ATS-GPU-BASE: GPU Streaming Library License + 1 Year Subscription	ATSGPU-001
ATS-GPU-OCT: Signal Processing Library License + 1 Year Subscription (requires ATSGPU-001)	ATSGPU-101
ATS-GPU-NUFFT: ATS-GPU-OCT Extension for fixed-frequency sampled data License + 1 Year Subscription (requires ATSGPU-001 & ATSGPU-101)	ATSGPU-201
5 Hours of technical support	SUPPORT-HR5

Manufactured By:

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DATASHEET REVISION HISTORY

Changes from version 1.3M (Dec 2023) to version 1.3N	Section, Page
Added section on ATS9625: Sync 4X1G	Multi-board Systems using ATS 4X1G, pg. 4
Modified warranty reinstatement fee information	Extended Warranty, pg. 8
Specified that Operating temperature is ambient	Environmental, pg. 10
Added Sync 4X1G, its accessories and extended warranty: ATS9625-025, SYNC-X1G-PWR, SYNC-4X1-CBL, SYNC-4X1-061	Ordering Information, pg. 11

Changes from version 1.3L (Apr 2023) to version 1.3M	Section, Page
Corrected unsigned binary positive full scale to 2^n-1 (was incorrectly stated as 2^{n-1}-1), corrected signed binary positive full scale to 2^{n-1}-1 (was incorrectly stated as 2^{n-2}-1) and negative full scale 2^{n-1} (was incorrectly stated as 2^{n-2}).	Output Data Format, pg. 5
Added paragraph on Boxcar Averaging for *ATS-GPU-BASE*	ATS-GPU, pg. 6
Modified to include new warranty reinstatement policy	Extended Warranty, pg. 7
Added section for REACH Compliance	REACH Compliance, pg. 8
Absolute maximum input: Corrected label for External Trigger from EXT to TRIG IN	Acquisition System, pg. 9
Trigger Engine Source: Corrected label for External Trigger from EXT to TRIG IN	Triggering System, pg. 10
Added REACH Compliance, CE Marking, and FCC Part 15/ICES-003 to list	Certification and Compliances, pg. 10

Changes from version 1.3K (Nov 2022) to version 1.3L	Section, Page
Added note to advise that ATS9625 is not recommended for new designs Suggested replacement is ATS9428 or ATS9628	pg. 1

Changes from version 1.3J (July 2022) to version 1.3K	Section, Page
Removed 32-bit Windows	Feature Table, pg. 1
Added new section to specify default output data format is unsigned binary and that it can be changed to signed binary via an API call.	Output Data Format, pg. 5
Separate description for Linux SDK to detail supported programming languages	Software Development Kits, pg. 6
Noted that only 64-bit Windows is supported and that the last driver version that supports 32-bit Windows is 5.10.24.	Support for Windows, pg. 7
Updated download link for the Linux driver and associated library, and added note: ATS-SDK example programs are only provided for Python and C++	Linux Support, pg. 7
Added new section to detail AlazarTech's accessory policy	Accessories for Out-of-Warranty Products, pg. 7
Added new section to detail AlazarTech's upgrade policy	Upgrading Your Digitizer in The Field, pg. 7
Removed "2G" from product names for ATS9625-002 & ATS9625-003	Ordering Information, pg. 10

Changes from version 1.3I (Nov 2021) to version 1.3J	Section, Page
Updated block diagram: Changed term for multi-board system to Leader/Follower Removed elements related to discontinued ATS962x Coprocessor FPGA Development Kit	ATS9625 block diagram, pg. 2
Removed NPT footers; this feature is not available on ATS9625	No Pre-Trigger (NPT) AutoDMA, pg. 3
Changes to maintenance subscription inclusions: removed technical support	Software Development Kits, pg. 6
Added Windows 11	Support for Windows, pg. 7
Added new section to specify how AlazarTech handles technical support: Customers receive free technical support on hardware products that are under warranty. Out-of-warranty support requires the purchase of support hours.	Technical Support, pg. 7
Updated Electromagnetic Immunity standard number (product was retested)	EC Conformity, pg. 8
Updated specification name from *Input protection* to *Absolute maximum input* Actual value did not change.	Acquisition System, pg. 9
Updated name for product *Software Development Kit* Now called: *ATS-SDK purchased with a digitizer board or ATS-GPU*	Ordering Information, pg. 10
Added products ATS-SDK-WOD and SUPPORT-HR5	Ordering Information, pg. 10

Changes from version 1.3H (Oct 2021) to version 1.3I	Section, Page
Changed term for multi-board system to *Leader/Follower*	Leader/Follower Systems, pg. 4
Specified number of extended warranties that users may purchase	Extended Warranty, pg. 7

DATASHEET REVISION HISTORY

Changes from version 1.3G (June 2021) to version 1.3H	Section, Page
Updated support status for Windows 8.x and Windows Server versions 2012 R2, 2016, 2019	Support for Windows, pg. 7
Updated Linux Support: only 64-bit Linux operating systems are supported	Linux Support, pg. 7
Changed terminology from *Information Technology Equipment (ITE)* to *Multimedia Equipment (MME)*	EC Conformity, pg. 7

Changes from version 1.3F (Jan 2020) to version 1.3G	Section, Page
Updated section *ATS-GPU* and added paragraph on ATS-GPU-NUFFT	ATS-GPU, pg. 6
Updated Linux Support (RHEL) and added new DKMS drivers	Linux Support, pg. 7
Updated product registration URL	Extended Warranty, pg. 7
Updated standards and directives	EC Conformity, pg. 7
Updated year of ICES-003 standard	FCC & ICES-003 Compliance, pg. 8
Added Auxiliary I/O input coupling (DC)	Auxiliary I/O (AUX I/O), pg. 10
Updated software descriptions and added order number for ATS-GPU-NUFFT	Ordering Information, pg. 10

Changes from version 1.3E (May 2019) to version 1.3F	Section, Page
Removed references to External Clock being optional. It is included with ATS9625.	Global change
Changed *Sampling Rate* column to *Max. Sample Rate*	Feature Table, pg. 1
Added AlazarFrontPanel (for Linux) as benchmarking tool	Maximum Sustained Transfer Rate, pg. 2
Replaced signal sine wave requirement with high slew rate for external clock signal	External Clock, pg. 5
Removed qualified metrology lab as option for recalibrating ATS9625	Calibration, pg. 6
Specified Windows 7 version support, re-ordered list of operating systems, and added end-of-support notice for Windows 7 and Windows Server 2008 R2	Support for Windows, pg. 6
Specified Linux distributions: CentOS, Debian, and Ubuntu	Linux Support, pg. 6
Changed fast external clock signal minimum amplitude from 200 mV_{P-P} to 500 mV_{P-P} Removed sine or square wave requirement for Signal Level Removed maximum amplitude, spec included in signal level	Fast External Clock Input, pg. 8
Changed 10 MHz Reference signal minimum amplitude from 200 mV_{P-P} to 500 mV_{P-P} Removed sine or square wave requirement for Signal Level	10 MHz Reference PLL Input, pg. 8
Corrected Output types (removed Busy Output and added Pacer Output)	Auxiliary I/O (AUX 1), pg. 9

Changes from version 1.3D (Apr 2019) to version 1.3E	Section, Page
Updated ATS-GPU benchmarks (FFTs per second, number of channels, and GPU)	ATS-GPU, pg. 6
Added section *Extended Warranty*	Extended Warranty, pg. 7
Updated effective date of the new Export Control Handbook (May 17, 2019)	Export Control Classification, pg. 7
Updated Trademark information	pg. 9

Changes from version 1.3C (Sept 2018) to version 1.3D	Section, Page
Removed references to the user-programmable FPGA and related FPGA Development Kit as the FPGA Development Kit is being discontinued	Global change
Updated block diagram to indicate Coprocessor FPGA model for each ATS9625 model	Block diagram, pg. 2
Updated *Optional High Capacity Coprocessor FPGA* section: larger Coprocessor FPGA is no longer available as an upgrade, users must order ATS9625-2G-SE260 in order to have the high-capacity P3SE260H780C4N Coprocessor FPGA	High-Capacity Coprocessor FPGA, pg. 3
Removed *ATS-GMA* section as this product is being discontinued	ATS-GMA, pg. 7
Specified that listed Pre-trigger depth applies to NPT mode	On-Board Acquisition Memory System, pg. 9
Removed ATS9625-013, ATS9625-FDK, ATSGMA-001, ATSGMA-101	Ordering Information, pg. 10
Added Windows Server to Trademark information	pg. 10

Changes from version 1.3B (Jan 2018) to version 1.3C	Section, Page
Updated RoHS Compliance to RoHS 3	Global change
Updated product image	pg. 1
Clarified Operating System Support	Feature Table, pg. 1
Updated *Recommended Motherboards or PCs*	Recommended Motherboards or PCs, pg. 3

DATASHEET REVISION HISTORY

Changes from version 1.3B (Jan 2018) to version 1.3C (continued)	Section, Page
Added AUX connector configurations for AUX 1 and AUX 2	AUX Connectors, pg. 6
Added information on ATS-SDK license	Software Development Kits, pg. 6
Specified 64-bit version for Windows and Linux support	ATS-GPU, pg. 7
Added *ATS-GMA* section	ATS-GMA, pg. 7
Added list of supported Microsoft Windows versions	Support for Windows, pg. 7
Added *Acquisition Memory System* section	Acquisition Memory System, pg. 9
Added Maximum Amplitude: 2 V_{P-P}	Optional ECLK (External Clock) Input, pg. 9
Added "PLL" to section name for clarity, corrected Input Frequency tolerance, and added Max. and Min. Frequencies	Optional 10 MHz Reference PLL Input, pg. 9
Corrected Trigger Engine Combination	Triggering System, pg. 10
Added *Auxiliary I/O (AUX 1)* section	Auxiliary I/O (AUX 1), pg. 10
Edited *TRIG OUT Output* section title to include *(AUX 2)*	TRIG OUT Output (AUX 2), pg. 10
Added subscription length for ATS-SDK, ATSGPU-001, ATSGPU-101 Added products ATSGMA-001, ATSGMA-101	Ordering Information, pg. 10
Added Trademark information	pg. 10

Changes from version 1.3A (Oct 2017) to version 1.3B	Section, Page
Added note about NPT Footers	No Pre-Trigger (NPT) AutoDMA, pg. 4
Added CNRC as calibration standard	Calibration, pg. 6
Added -BASE and -OCT to ATS-GPU description for clarity	ATS-GPU, pg. 6
Corrected size of card	Physical, pg. 9
Updated email address	Manufactured By, pg. 10

Changes from version 1.3 (Sept 2017) to version 1.3A	Section, Page
Added bandwidth for optional Wideband Upgrade	Feature Table, pg. 1
Added Wideband Input section	Wideband Input Upgrade, pg. 6
Added Bandwidth with Wideband Upgrade	Acquisition System, pg. 9
Updated description for product ATSGPU-001 & ATSGPU-101	Ordering Information System, pg. 10

Changes from version 1.1C (Jan 2013) to version 1.3	Section, Page
Added Python to list of SDK supported languages, and Support for Windows & Linux	Features, pg. 1
Added Python & LabVIEW to list of supported languages for ATS-SDK, removed ATS-VI	Overview, pg. 1
Added 2-slot-spacing SyncBoards (-W models)	Master/Slave Systems, pg. 4
Added section on External Trigger Input	External Trigger Input, pg. 5
Modified AlazarDSO description	AlazarDSO Software, pg. 6
Updated ATS-SDK description: added Python, removed ATS-VI	Software Development Kits, pg. 6
Replaced *GPU Based Signal Processing* section with new *ATS-GPU* section	ATS-GPU, pg. 6
Replaced section *ATS-Linux* with *Linux Support*; now includes download link & updated description	Linux Support, pg. 6
Added Export Control Classification information	Export Control Classification, pg. 7
Added section on RoHS compliance	RoHS Compliance, pg. 7
Added section on EC Conformity	EC Conformity, pg. 7
Added section on FCC & ICES-003 Compliance	FCC & ICES-003 Compliance, pg. 7
Updated External Trigger Input Impedance to 6.4 kΩ ±10%	TRIG IN (External Trigger) Input, pg. 10
Updated list of Certification and Compliances	Certification and Compliances, pg. 10
Corrected product name for ATS-SDK	Ordering Information, pg. 10
Removed products ATS-VI (ATS-SDK now supports LabVIEW), ATS9625-LIN	Ordering Information, pg. 10
Added products ATS9625-012, ATS9625-020, ATS9625-021, ATS9625-022, ATS9625-061, ATS9625-062, ATSGPU-001, ATSGPU-101	Ordering Information, pg. 10